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Fluxless silicon-to-alumina bonding using electroplated Au–Sn–Au structure at eutectic composition

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Abstract

Large 6 mm × 9 mm silicon chips have been successfully bonded to alumina substrates with electroplated Au/Sn/Au structure at the eutectic composition. The new bonding process is entirely fluxless, or flux-free. It is performed in vacuum (50 milliTorrs), where the oxygen content is reduced by a factor of 15,200 comparing to air, to inhibit solder oxidation. Eutectic Au80Sn20 alloy is a well established solder that exhibits excellent fatigue-resistance, creep-resistance, and long-term reliability. Despite the popularity of plastic packages and organic substrates, alumina remains an important packaging material for highly reliable products in demanding environment. A major challenge in silicon-to-alumina bonding is the large thermal expansion mismatch between silicon (2.7 ppm/°C) and alumina (7 ppm/°C). The new process developed shows that a large silicon chip can be bonded to an alumina substrate without chip cracking or solder fracture. In this research, we learned the specific bonding procedures necessary to turn the Au/Sn/Au structure into homogeneous eutectic alloy without the chip breaking away from the solder layer. Nearly void-free joints are produced as confirmed by a scanning acoustic microscope (SAM). The joints are studied using scanning electron microscope (SEM) and energy dispersive X-ray spectroscopy (EDX) to evaluate the microstructure and the composition.

Keywords: Fluxless bonding; Fluxless soldering; Soldering; Eutectic Au–Sn alloys; Electroplating

1. Introduction

Even though the plastic package is the most widely used package for semiconductor devices, the ceramic package is still important for devices requiring high reliability and for devices that need to be hermetically sealed [1]. There are many devices that use hermetic sealed ceramic packages such as MEMS, sensors, microwave devices, and imaging devices [2–4]. Common ceramic packaging materials are composed of more than 90% alumina and have a nominal coefficient of thermal expansion of 7 ppm/°C. Attaching large silicon chips to ceramic packages has been a serious challenge because of thermal expansion mismatch between silicon of 2.7 ppm/°C and alumina of 7 ppm/°C. Attaching the chip using silver epoxy is not generally accepted due to possible outgassing and low thermal conductivity. An alternative is to use popular soft solders such as Sn–Pb, Sn–Ag, and Sn–Cu. However, these soft solders are likely to incur thermal fatigue, leading to long-term reliability problems [5,6]. The fatigue is caused by the extreme plastic shear strains exerted on the solder layer as a result of large chip area and thermal expansion mismatch. One way to reduce the fatigue is to use hard solders. The most commonly used hard solder is the eutectic Au80Sn20 alloy. For decades, it has been employed to hermetically seal a ring or lid to a package [7,8] and to attach laser diode chips [9]. It is widely used in photonic packaging. It is known to possess high yield strength, high resistance to fatigue, and high resistance to creep [5,10]. The joints made of AuSn eutectic have been shown to achieve exceptional long-term reliability. In bonding large silicon chips to alumina substrates using eutectic AuSn solder, the challenge is to manage the thermal expansion mismatch. Since the range of plastic strain of AuSn eutectic is very small, the resulting joint must be nearly void-free and the interfaces must be strong to withstand the stresses developed in the bonded structure. We had previously bonded 6 mm × 10 mm

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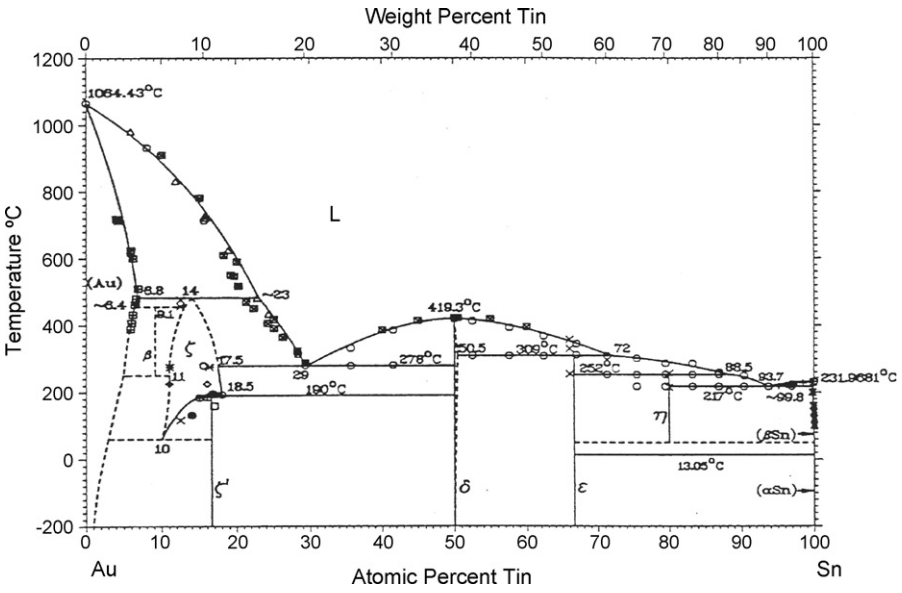

Fig. 1. Tin–gold phase diagram [14].

silicon chips on alumina substrates using Au–Sn preform without any scrubbing action and without any flux [11]. The bonding process was performed in H_2 environment to inhibit oxidation. While the Au-Sn eutectic preform works, it is hard to pick and place the preform onto the bond pad. It is also difficult to control the thickness of the bonding layer. Thus, vacuum deposition is introduced to fabricate the Au/Sn/Au structures for fluxless bonding where oxidation is inhibited in solder production as well as during the boding process [12].

In this research, we look into electroplating processes to fabricate Au/Sn/Au solder structures directly on alumina substrates. The primary reason is cost reduction. The secondary reason is the possibility of solder patterning using photolithographic process. The third one is the ability to deposit on places not accessible with vacuum deposition technique. The solder structure is so designed that the bonding process can be performed without the use of any flux. Fluxless feature is critically important in achieving void-free joints in bonding large chips because flux and flux residues can be easily trapped in the joint, causing voids. Fluxless technique has become important in packaging MEMS and photonic devices that simply cannot be exposed to flux. In some applications, flux residues could cause reliability problem [13]. The newly developed fluxless process is performed in a vacuum chamber pumped to 50 milliTorrs to suppress tin oxidation. In this vacuum range, the oxygen content is reduced by a factor of 15,200 comparing to that in air. This is in contrast to our previous processes that were performed in H_2 environment [11,12]. The change from H_2 environment to vacuum is motivated by our future needs to package sensor device chips inside a vacuum condition.

In what follows, we briefly review gold–tin binary system to help explain the structure designs and the bonding principle. Solder designs and bonding procedures are presented. Experimental results are reported and discussed. A short summary is then given.

2. Gold–tin binary system

To help explain the multilayer solder designs and bonding principle, we briefly review the gold–tin phase diagram exhibited in Fig. 1 [14,15]. It depicts a complex combination of eutectic and peritectic systems. There are five intermediate phases: ζ phase, Au_5Sn, AuSn, $AuSn_2$, and $AuSn_4$. The ζ phase (hexagonal close-packed crystal structure) is homogeneous between 12 and 16 at.% Sn. The intermetallic compound AuSn (hexagonal NiAs structure) has a very narrow range of solubility. The homogeneity range of $AuSn_2$ (orthorhombic) and $AuSn_4$ (orthorhombic $PtSn_4$ structure) are also very narrow. The liquid phase is identified as L. The $L \leftrightarrow [\zeta + AuSn]$ eutectic occurs at 278 °C with 29.5 at.% Sn. This is the most commonly used eutectic composition of 20 wt.% Sn and 80 wt.% Au. The δ phase is determined as the AuSn intermetallic that has a melting point of 419.3 °C. The homogeneity range extends from 50.0 to 50.5 at.% Sn. The ε phase is identified as the $AuSn_2$ intermetallic compound. The temperature of the peritectic $[L + \delta] \leftrightarrow \varepsilon$ reaction is 309 °C, giving the liquidus composition of about 72 at.% Sn. The homogeneity range of this phase is very narrow. The η phase is the $AuSn_4$ compound. The temperature of the peritectic $[L + \varepsilon] \leftrightarrow \eta$ reaction is 252 °C, giving the liquidus composition of about 88.5 at.% Sn. The $L \leftrightarrow [\eta + \beta Sn]$ eutectic reaction occurs at 93.7 at.% Sn at 217 °C, called as second eutectic reaction. Lastly, the allotropic temperature between two terminal solid solutions of (β-Sn) and (α-Sn) is 13.05 °C. The (β-Sn) solid solution has a solubility up to 0.2 at.% Au in β-Sn. The (α-Sn) solid solution has a very limited solid solubility, that is, less than 0.006 at.% Au in α-Sn.

3. Experiment procedure and bonding process designs

To perform fluxless bonding, thin Cr layer of 0.03 μm and Au layer of 0.1 μm are deposited on a Si wafer in a high

vacuum e-beam evaporator (3×10^{-6} Torr). Cr acts as an adhesion layer and the Au layer is to prevent Cr oxidation. The wafer with Cr/Au layers is diced into 6 mm × 9 mm pieces using Tempress dicing saw. Alumina substrate with Ti/W/Au metallization is first electroplated with 11 μm of Au. The Au plating bath is neutral non-cyanide plating solution at pH 7 based on sulfite complex with mild agitation. The current density and process temperature are 4.6 mA/cm^2 and 60 °C, respectively. It is then followed by 7.5 μm of Sn plated in a stannous tin based bath at 21.5 mA/cm^2. Very thin Au capping layer (0.1 μm) is plated over the Sn layer mainly to prevent oxidation of the Sn. The finished alumina substrate is diced into 10 mm × 12 mm pieces. The Si chip and alumina substrate are held together in a graphite boat with 50 psi (0.35 MPa) static pressure to ensure intimate contact. The boat is then fastened on the graphite platform inside a vacuum chamber built in house. The chamber is pumped down to 50 milliTorrs and the platform is heated to the desired temperature using a temperature controller. Temperature of the sample is measured and monitored with a thermocouple.

Three different bonding processes are designed and implemented. For the first design, the sample on the platform is heated to 320 °C for 12-min duration above 280 °C. The sample is then allowed to cool naturally to room temperature in vacuum condition. For the second design, the bonding temperature is increased to 430 °C in the vacuum chamber with a dwell time of 5 min. Reason for choosing this temperature will be explained in the next section. For the third design, the alumina substrate with Au/Sn/Au plated structure first undergoes a reflow process at 430 °C to convert the Au/Sn/Au multilayer structure into uniform eutectic layer. The silicon chip is then bonded to the alumina substrate at 320 °C. No flux is used in these three processes. To evaluate the quality of the joints, SAM is used to identify voids in the solder joints. SEM and EDX are employed to characterize the composition and microstructures of solder joints. The re-melting temperature of several samples is measured by specially designed de-bonding test tool.

4. Experimental results

4.1. The first bonding process design—the 320 °C process

For the first design presented in the previous section, the bonding temperature was chosen as 320 °C, typical for bonding processes using Au–Sn eutectic alloys. The Si chip with Cr/Au and alumina substrate with Ti/W/Au and electroplated Au/Sn/Au solder structure were held together with static pressure of 50 psi (0.35 MPa) and heated to 320 °C for 12-min reflow time, i.e. duration above the expected melting temperature of 280 °C, and allowed to cool naturally to room temperature in vacuum environment. After the sample was taken out of the vacuum chamber, it was found that the Si chip did not bond well to the alumina substrate. The same process was tried many times with the similar result. To investigate the clue, we used SEM and EDX analysis to evaluate the fracture surface and fracture mode. Fig. 2 displays secondary electron images of the Si chip and of the alumina substrate, respectively, of a typical sample. EDX data are presented in Tables 1 and 2, respectively. The SEM image of the silicon chip shows dark background with small bright patches. On the dark region, EDX analysis detects mostly Si and low Cr signal. The bright patches consist of mainly Sn with some Au. Thus, we can see that the silicon chip broke

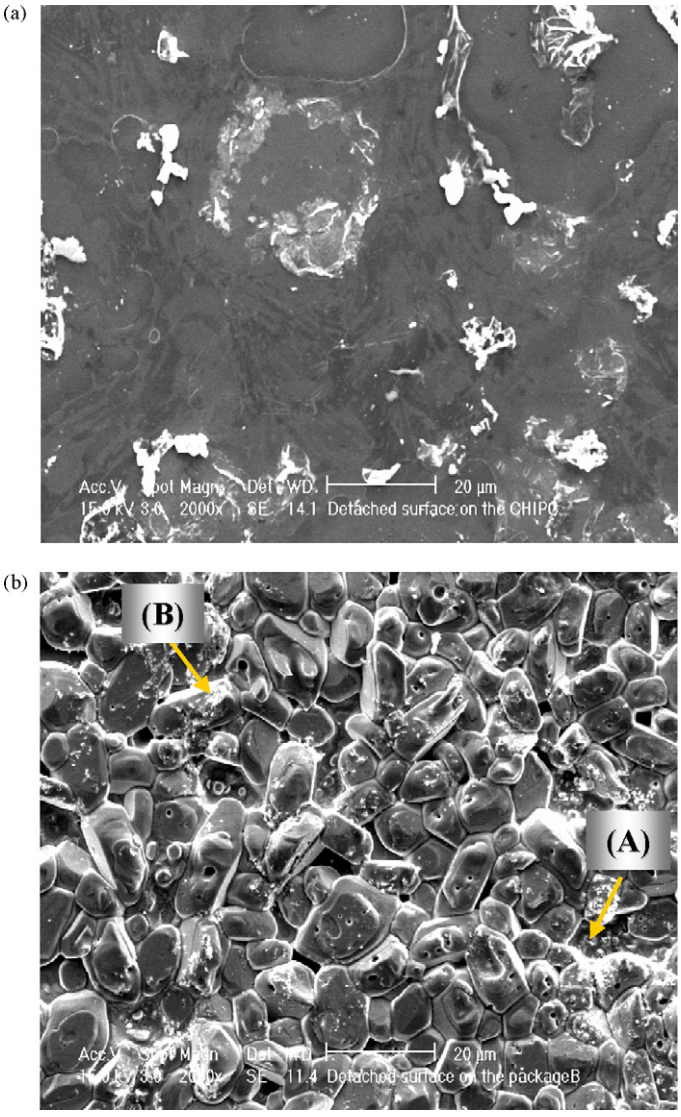

Fig. 2. SEM images of a sample bonded with 320 °C processes: (a) detached Si chip (b) detached alumina substrate.

Table 1
EDX spectra on broken silicon surface

Si side	at.%
(a) Dark background	
Si	96–98
Cr	2–4
(b) Bright patches	
Si	37–42
Sn	36–40
Au	10–13
Cr	7–8

Table 2
EDX spectra on broken alumina surface

Alumina side	at.%
Bright patches	
Region A	
Au	≅33
Sn	≅66
Region B	
Au	≅20
Sn	≅80
Granular region	
Au	43–47
Sn	52–55

mostly along the interface between Si/Cr and Au–Sn solder, with small patches of Au–Sn solder staying on it. Notice that the Si chip was coated with Cr/Au which looked golden shining before bonding. After it broke away from the alumina substrate during the bonding process, EDX analysis did not detect any gold element. The surface looked silvery rather than golden under optical microscope. These observations indicate that the molten Au–Sn phase on the alumina did wet and react with the thin Au layer on the Si chip during the bonding process. It is during the reaction phase or cooling phase that the Si chip broke along the interface between the Cr on Si and the Au–Sn solder on alumina substrate. The reason of breakage is presented in the next paragraph.

On the alumina substrate, distinct granular structure is observed. Table 2 displays EDX results in three different regions. Based on the EDX data and the phase diagram in Fig. 1, we can judge that the grains are mostly AuSn compound with some $AuSn_2$ or $AuSn_4$ compounds. No β-Sn phase exists. We explain what happened as follows, with the help of Fig. 3. Fig. 3(a) depicts the silicon chip and the alumina substrate before bonding. At 320 °C bonding temperature, the Sn layer in the Au/Sn/Au structure on the alumina substrate melted and dissolved the thin outer Au layer completely and reacted with the thick Au layer beneath it to form the (L) phase shown in the phase diagram (Fig. 1). The overall composition of the Au/Sn/Au structure was designed to be near eutectic. Thus, the Au composition of the (L) phase increased as the reaction continued. The (L) phase eventually moved below the liquidus line between the AuSn phase and $AuSn_2$ phase and turned into molten phase with AuSn compound grains. When it got close to the AuSn phase, the amount of the molten phase became small comparing to the AuSn solid grains. The molten phase is not enough to occupy the gap between the AuSn grains and the Cr layer on the Si chip, as illustrated in Fig. 3(b). This gap was created due to the solidifying AuSn grains. The existence of this gap made it easy for the Si chip to break from the alumina substrate as a result of thermal expansion mismatch during the cooling phase of the process, as exhibited in Fig. 3(c). According to the phase diagram, the molten phase should consist of $AuSn_2$ and $AuSn_4$ grains upon cooling down to room temperature, which was confirmed by the EDX data in Table 2.

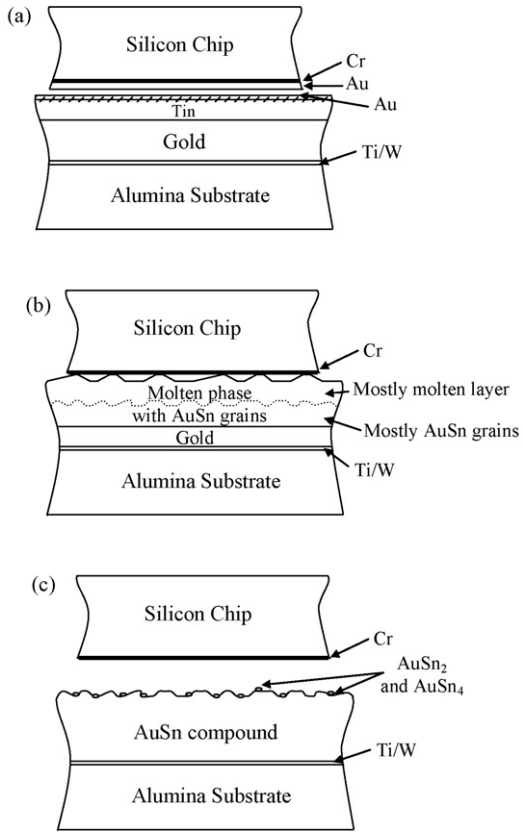

Fig. 3. Reactions of the fluxless 320 °C Au–Sn bonding process. (a) Before bonding; (b) at bonding temperature of 320 °C; (c) after cooling down to room temperature.

With the above understanding, we see that, to avoid the breakage of the Si chip from the alumina substrate, the solid content of the solder material during the dwell time of the bonding process must be reduced to a minimum. The melting temperature of the AuSn compound (δ phase) is 419 °C. If we increase the bonding temperature above 419 °C, the solder material will stay completely in molten phase during dwell time. This argument guides us towards the next two bonding designs.

4.2. The second bonding process design—the 430 °C process

Based upon the results and discussion of the 320 °C bonding process presented above, we decided to try a bonding temperature of 430 °C to verify our design principle. Four hundred and thirty degree Celsius is above the 419 °C, the melting temperature of AuSn compound. The dwell time used is 5 min. Based on the Au–Sn phase diagram, Fig. 1, the Au/Sn/Au multilayer solder structure at eutectic composition on the alumina substrate would turn into the molten (L) phase during the bonding process, as illustrated in Fig. 4. After cooling down to room temperature, the joint eventually solidifies at the Au80Sn20 eutectic composition. The process is entirely fluxless. Nearly void-free joints were indeed achieved, as confirmed by a scanning acoustic microscope (SAM).

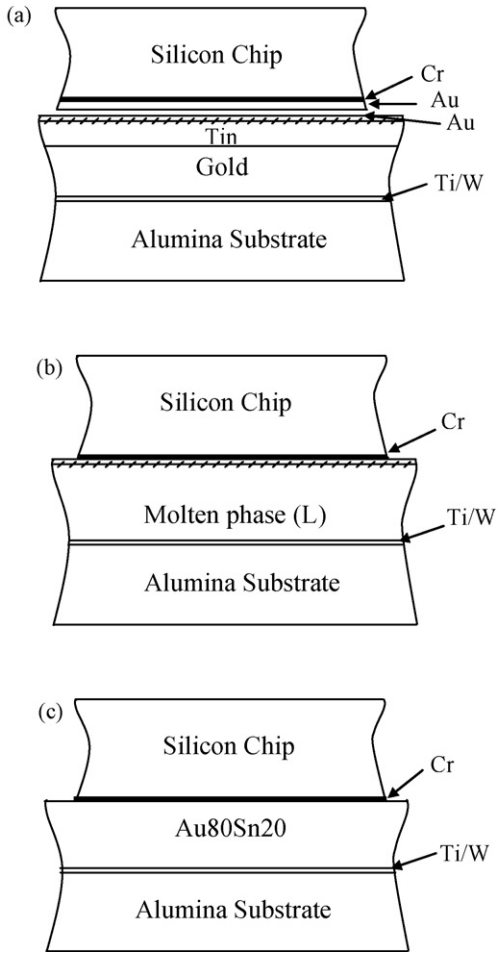

Fig. 4. Principle of the fluxless 430 °C Au–Sn bonding process. (a) Before bonding; (b) at bonding temperature of 430 °C; (c) after cooling down to room temperature.

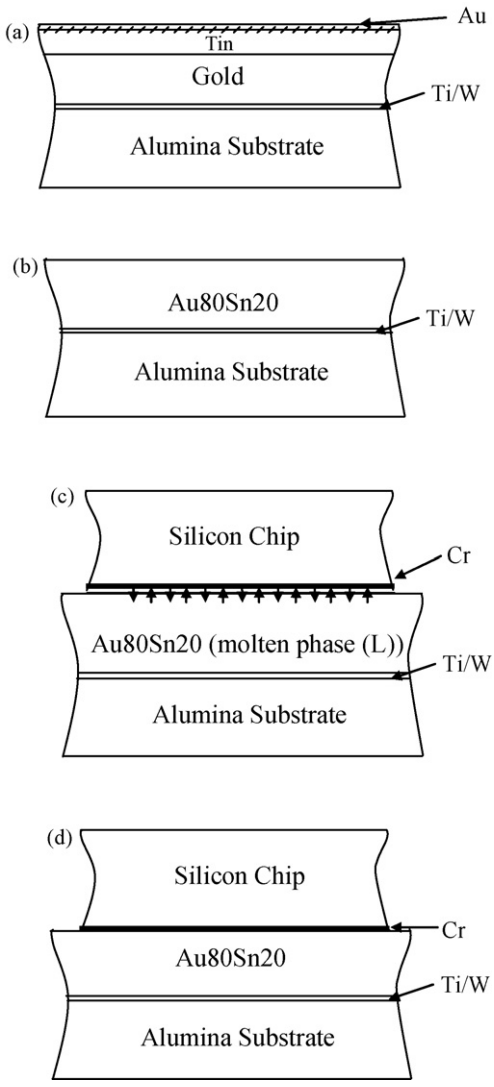

Fig. 5. Principle of the fluxless Au–Sn bonding at 320 °C after 430 °C reflow process. (a) Before reflow; (b) after 430 °C reflow process; (c) during bonding at 320 °C; (d) after cooling to room temperature.

4.3. The third bonding process design—320 °C process after 430 °C reflow

For many devices, the 430 °C bonding temperature of the second design presented above is too high and a lower temperature process is needed. We thus came up with third fluxless design, as illustrated in Fig. 5. The Au/Sn/Au structure electroplated on the alumina substrate was reflowed at 430 °C to convert it to homogeneous eutectic Au80Sn20 alloy. Alumina packages and substrates can easily sustain this solder reflow temperature. The process was performed in the vacuum chamber to inhibit oxidation. After reflow, the eutectic alloy has a melting of 280 °C. The silicon chip was then bonded to the alumina substrate at 320 °C without using any flux. The resulting joints are nearly void free. The bonding layer consists of near eutectic Au80Sn20 alloy.

4.4. Experimental analyses and de-bonding test

The samples produced by the 430 °C bonding process and the 320 °C bonding process after 430 °C reflow exhibit similar quality. Fig. 6 displays secondary electron images of a typical joint produced by 430 °C bonding process at lower magnification (a) and higher magnification (b). The bonding layer is very uniform with a thickness of 3 μm. Due to static pressure applied to hold the chip and substrate in intimate contact, significant amount of solder material was squeezed out during the bonding process. The bonding layer thus was thinner that the original Au/Sn/Au structure on alumina. In packaging applications, the thickness can be controlled by using small spacers or by adjusting the static pressure. Table 3 shows the EDX data of the joint. The composition is not exactly eutectic Au80Sn20, but rather is Au-richer than eutectic. This is likely caused by the molten solder being squeezed out during bonding, making the material retained in the bonding layer richer in gold.

Table 3
EDX spectra of AuSn solder joint

	wt.%
Au	83–86
Sn	14–17

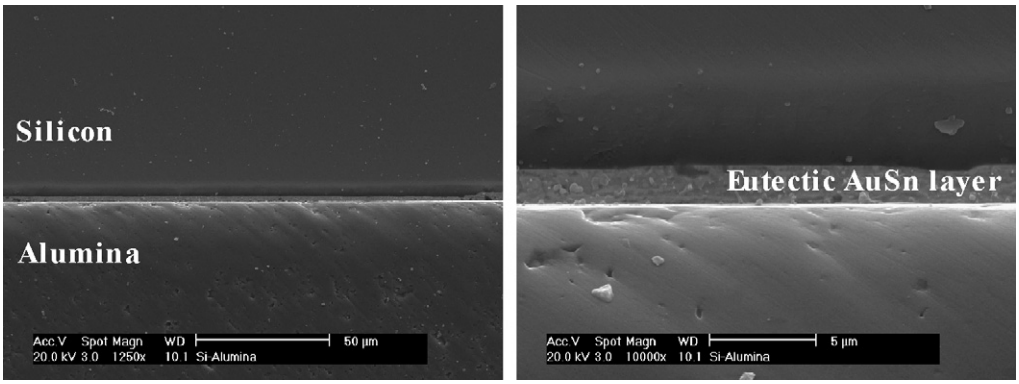

Fig. 6. SEM images on the cross section of a silicon chip bonded to an alumina substrate using Au–Sn eutectic alloy: (a) low magnification (1250×) and (b) high magnification (10,000×).

The quality of joints is examined by a transmission-type SAM (Sonix HS 1000) at an operating frequency of 15 MHz. Fig. 7 exhibits the SAM image of a typical sample. It is nearly void-free. For specific type of samples like these where relatively high stress is induced in the joint due to thermal expansion mismatch between silicon and alumina, void-free quality is important. Voids can induce localized and concentrated stresses on the silicon chip, resulting in chip breakage or cracking. The solder joints produced using either processes, 430 °C bonding process or 320 °C process after 430 °C reflow, are very strong. We tried very hard to break several samples with a hand tool but the silicon chip always broke first.

Melting temperature of the samples made by the 430 °C bonding process or the 320 °C process after 430 °C were tested using specially designed de-bonding fixture. A small shear force is applied to the chip and the sample is heated in an oven while the temperature is monitored. The temperature is recorded when the chip detaches from the substrate. Results of four samples give a melting temperature between 272 and 279 °C, which is quite close to the melting point of the eutectic AuSn alloy. Even thought the composition is not exactly at the eutectic composition, the alloy would start to melt at the 278 °C solidus temperature shown in the phase diagram (Fig. 1).

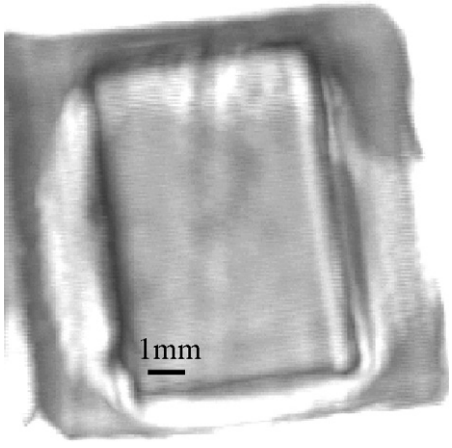

Fig. 7. SAM image of a sample of Si chip bonded to alumina substrate with Au–Sn eutectic joint.

5. Summary

In summary, we have successfully developed a fluxless bonding process between silicon chips and alumina substrates. Electroplating processes were employed to manufacture Au/Sn/Au multilayer structure at eutectic Au–Sn composition to produce fluxless joints of high quality. The electroplated Au/Sn/Au structure on alumina substrates turned into homogeneous eutectic Au–Sn alloy either by a 430 °C bonding process or by a 430 °C reflow process before bonding at 320 °C. Despite the significant thermal expansion mismatch between silicon and alumina, large silicon chips of 6 mm × 9 mm were bonded to alumina substrates without any cracking. The resulting Au–Sn joints are nearly void free. The silicon chip could not be detached from the substrate using a hand tool. The chip always fractured first. These new fluxless processes using electroplated Au/Sn/Au structures are valuable in hermetic lid sealing on ceramic packages, and in various packaging applications such as photonic devices, MEMS devices, sensor devices, and biomedical devices, where the use of flux is not an option.

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