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Single-mask fabrication of high-G piezoresistive accelerometers with extended temperature range

E Jesper Eklund and Andrei M Shkel

Microsystems Laboratory, University of California, Irvine, CA 92697, USA

E-mail: eeklund@uci.edu and ashkel@uci.edu

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Abstract
This paper presents a fabrication process in which all components of an in-plane piezoresistive accelerometer are fabricated simultaneously using a single mask. By dry-etching a silicon-on-insulator (SOI) wafer that has a specific resistivity, piezoresistors are defined and isolated from each other and from the bulk silicon without the pn-junctions normally required in piezoresistive sensors. In addition to simplifying the fabrication, the temperature range is also extended when compared to conventional piezoresistive accelerometers, due to the absence of pn-junctions. Single-axis accelerometers, designed for an acceleration range of 1 G to 500 G with a sensitivity of 1 mV G^{-1}, were fabricated and tested, and linear output characteristics were demonstrated. The temperature performance was also characterized. The temperature coefficient of sensitivity (TCS) was 0.3% $^{\circ}C^{-1}$ and the temperature coefficient of offset (TCO) was 20 mG $^{\circ}C^{-1}$.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Micromachined piezoresistive accelerometers were first demonstrated in the late 1970s by Roylance and Angell [1]. Their design was based on an anisotropically etched n-type (1 0 0) silicon proof mass that deflected out-of-plane. p-type piezoresistors were diffused into a beam that connected the proof mass to the surrounding bulk silicon, and the strain induced by applied acceleration led to a change in resistance which could be detected and related to acceleration. Several design improvements have since been proposed, including mechanical overrange protection [2], in-plane deflection of the proof mass [3], integrated detection circuitry [4, 5], formation of piezoresistors on etched sidewalls [6], temperature compensation [7] and different mass and suspension geometries (for example [3, 6, 8–11]). However, with the exception of [3], in which (1 1 0) silicon is anisotropically etched to achieve vertical sidewalls and the proof mass deflects in-plane, the conceptual design of most commercial piezoresistive accelerometers remains largely unchanged and can be traced back to the original design by Roylance and Angell [1].

In conventional piezoresistive accelerometers the piezoresistors and conductors are defined by doping selected areas of a silicon wafer to achieve pn-junctions. At least two doping steps are employed in order to obtain both heavily doped conductors and ohmic contacts, as well as lightly doped piezoresistors. Once the piezoresistors and conductors have been defined, additional fabrication steps are required to etch the suspension system as well as the free-standing proof mass. Thus, at least four photomasks are required during conventional fabrication, although a larger number of masks is often used in commercial processes.

Since pn-junctions are used to isolate the sensing elements from each other and from the bulk silicon in most piezoresistive accelerometers, leakage currents limit the operation of these sensors to about 150 °C [12]. Furthermore, the piezoresistive coefficients are highly dependent on temperature [13], leading to a change in sensitivity when piezoresistive sensors are operated at fluctuating temperatures. While the temperature coefficient of sensitivity (TCS) can be compensated for [14], the limited temperature range of piezoresistive silicon accelerometers can only be addressed by eliminating the pn-junctions. Silicon-on-insulator (SOI) wafers can be utilized

for this purpose. By defining the piezoresistors in the device layer and using the buried oxide to isolate them from the proof mass and the support structure in the handle layer, operational temperatures of 400 °C have been demonstrated [9].

Another drawback of many piezoresistive accelerometers is the out-of-plane deflection of the proof mass, necessitating cumbersome overrange stops above and below the structure to assure survival when the sensor is subjected to excessive accelerations. This is often accomplished by bonding of glass or silicon wafers to both sides of the device wafer. However, while most commercial piezoresistive accelerometers still deflect out-of-plane, several innovative designs of in-plane accelerometers have been demonstrated [3, 6, 10].

This paper describes a fabrication process for piezoresistive accelerometers that combines the improved temperature performance of SOI sensors with an in-plane design approach. Furthermore, the accelerometers are fabricated with a single photomask, greatly reducing the number of required fabrication steps compared to conventional piezoresistive accelerometers [15].

The fabrication process is based on deep reactive ion etching (DRIE) of the SOI device layer in order to simultaneously define piezoresistors, reference resistors, a proof mass, conductors, overrange stops, and a suspension beam. By choosing wafers with a particulary resistivity, piezoresistors can be achieved without pn-junctions and the doping steps can be eliminated from the fabrication process. Free-standing structures are obtained by selective removal of the buried oxide layer.

The presented accelerometers are designed to measure high G-loads. Some of the possible applications include airbag deployment systems, automotive crash testing, and munitions testing.

Section 2 describes the conceptual accelerometer design, discusses temperature issues, and introduces design parameters. The details of the fabrication process are then presented in section 3. Section 4 contains experimental results, including high-G and thermal characterization.

2. Accelerometer design

2.1. Design overview

The conceptual design of the single-mask piezoresistive accelerometer is illustrated in figure 1(*a*). All of the features are defined with one photomask and are etched simultaneously in the device layer of a single-crystal SOI wafer with a selected low resistivity, as will be described in section 3. The oxide layer underneath the proof mass is removed through the release holes using hydrofluoric (HF) acid, leading to a mass that is free to deflect in-plane. Areas without release holes, including bonding pads P_1, P_2, P_3 and P_4, define anchor points. A suspension beam attaches the proof mass to pad P_3 and two narrow piezoresistors are defined between the proof mass and pads P_1 and P_4. During applied acceleration, bending will occur around the centrally located suspension beam, causing one of the piezoresistors to stretch and the other one to compress. This leads to an increased resistance in the stretched piezoresistor and decreased resistance in the compressed piezoresistor. Overrange stops are etched on both sides of the proof mass to prevent breakage when the accelerometer is subjected to excessive accelerations.

The piezoresistive accelerometer is designed to emulate a Wheatstone bridge (compare to figure 1(*b*)). A half-bridge configuration is chosen with the piezoresistors (R_3 and R_4) on the right-hand side of bonding pads P_1 and P_4 and the reference resistors (R_1 and R_2) on the left-hand side.

In order to amplify the output voltage, a signal conditioning circuit can potentially be integrated with the accelerometer on the SOI chip. Alternatively, a two-chip solution can be used, where the signal conditioning circuit is located on a separate chip and wire-bonded to the pads of the accelerometer bridge circuit.

Since the only difference between the piezoresistors and the reference resistors in figure 1(*a*) is that the piezoresistors are free to deform when the proof mass deflects, while the reference resistors are anchored, the resistance will change equally with temperature on both sides of the bridge and no significant change in the output voltage due to temperature is expected. There will however be a slight change in sensitivity due to the temperature dependence of the piezoresistive coefficients, discussed in the next section.

Although the suspension beam is preferably much wider than the piezoresistors and reference resistors, it still has a small resistance and a slight voltage drop is therefore expected. In order to maintain a symmetrical and balanced Wheatstone bridge, a similar structure is therefore included on the left-hand side. This structure is anchored on both sides between bonding pad P_2 and a wide conductor. Since the cross-sectional area of this wide conductor and the proof mass is much greater than the width of the piezoresistors and reference resistors, the voltage drop over the conductor and proof mass can be neglected.

The accelerometer is fabricated in a thick (preferably 50 μm–100 μm) device layer of an SOI wafer, and the width of the suspension beam is smaller than the thickness. This gives a structure that is stiff in the out-of-plane direction and compliant in the in-plane direction. However, even if the proof mass would deflect out-of-plane during excitation, the change in resistance would be equal for both piezoresistors and the voltage output would be unaffected, due to the half-bridge sensor configuration.

2.2. Principle of operation

The piezoresistive effect causes a change in resistivity, ρ, when a conductive material is subjected to stress. For the piezoresistors described in the previous section, the resistance is given by $R = \rho L_0/A$, where L_0 is the length and A the cross-sectional area. Assuming that the dimensional changes can be neglected and that the stress is applied in the longitudinal direction, the change in resistance, ΔR, is given by

$$\frac{\Delta R}{R_0} = \pi_l \sigma_l, \quad (1)$$

where R_0 is the initial resistance, π_l is the longitudinal piezoresistive coefficient and σ_l is the longitudinal stress [13]. The piezoresistive coefficients are dependent on the dopant concentration, crystal orientation, and temperature. At room temperature, the measured piezoresistive coefficients for p-type single-crystal silicon with a resistivity of 7.8 Ω cm are

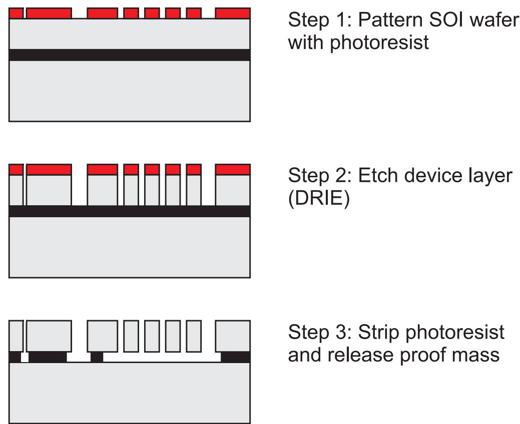

Figure 2. Single-mask SOI fabrication process for piezoresistive accelerometers.

accelerometers in order to optimize the design. Although most of the parameters in equation (7) can otherwise be chosen relatively freely, the choice of width of the piezoresistors is somewhat limited. The length of a piezoresistor can be expressed as $L_0 = R_0 w_{pr} h/\rho$, and it is preferred to make the piezoresistors as thin as possible to assure bending around the centrally located suspension beam. However, due to the limited aspect ratio of the DRIE (here assumed to be 25:1), the minimum width is approximately $w_{pr} = h/25$.

The accelerometer that will be considered in section 4 was fabricated from a 50 μm thick SOI device layer with a resistivity of 0.12 Ω cm. It was designed for an acceleration range of 1 G to 500 G, with $w_{pr} = 2$ μm, $d_{pr} = 60$ μm, $w_{beam} = 12$ μm and $L_0 = 38$ μm. The proof mass is 934 μm $\times$ 3735 μm, the etch holes are 15 μm $\times$ 15 μm, and the density of silicon is 2330 kg m^{-3}, leading to $m = 3.5 \times 10^{-7}$ kg and $d_{cg} = 1906$ μm. With a gage factor of $G = 121$ (estimated earlier in this section) and an applied voltage of $V_{in} = 5$ V, the sensitivity is estimated to be $S = 1$ mV G^{-1}. The natural frequency can be calculated as $f_n = 1/2\pi \times \sqrt{k/m} =$ 8.1 kHz.

3. Fabrication process

Multiple photomasks are normally required when fabricating piezoresistive accelerometers in order to define the piezoresistors, conductors, proof mass, and suspension system. By eliminating the need for doping steps, piezoresistive accelerometers are fabricated using only one photomask in the process described in this section.

The single-mask fabrication process depicted in figure 2 is based on SOI wafers with a specific resistivity. First, a layer of Shipley 1827 photoresist is spin-coated onto the wafer. The layout of the proof mass, suspension beam, thin piezoresistors, overrange stops, and wide conductors is then patterned using a photomask and the photoresist is exposed and developed. Next, deep reactive ion etching (DRIE) is utilized to etch the device layer of the SOI wafer all the way to the buried silicon oxide. The wafer is then diced and the photoresist is stripped. Finally, selected parts of the silicon oxide layer is removed with hydrofluoric (HF) acid and a free-standing proof mass is obtained. Areas without release holes define anchor points.

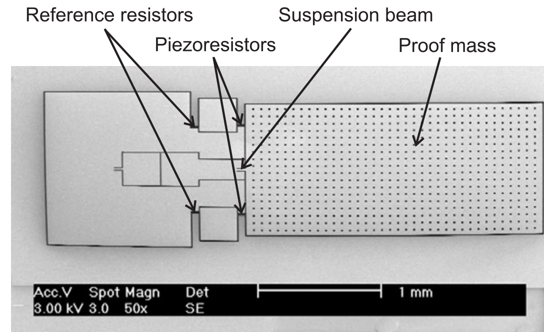

Figure 3. SEM image of a single-axis piezoresistive accelerometer.

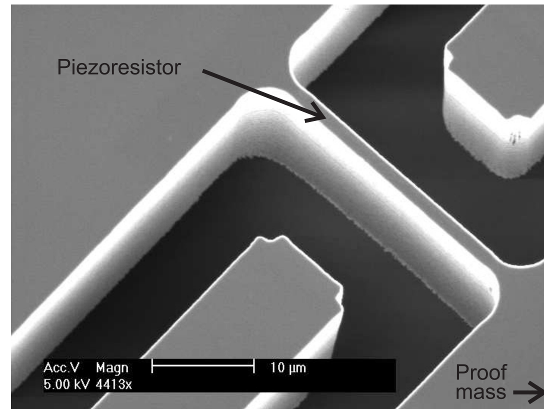

Figure 4. Close-up of a piezoresistor. The width is approximately 2 μm and the height 50 μm (SOI device layer).

Figure 3 shows a scanning electron microscope (SEM) image of a fabricated single-axis accelerometer. While the piezoresistors are attached to the proof mass, the reference resistors are anchored. Since the reference resistors are included on the chip and designed to be equal in size to the piezoresistors, all four resistors should have the same temperature properties. In contrast, in many traditional piezoresistive sensors off-chip reference resistors are used, often requiring additional temperature compensation in order to adjust for temperature dependence of the sensitivity and the voltage offset.

It is expected that the proposed fabrication process will allow for higher operational temperatures than sensors where pn-junctions are used to isolate the piezoresistors, due to high leakage currents in pn-junctions above 150 °C. Note, however, that while the presented SOI sensors will likely be operational up to about 350 °C, temperature compensation of the sensitivity will still be required due to the temperature dependence of the piezoresistive coefficients, discussed in section 2.

Figure 4 displays a close-up SEM image of one of the 2 μm wide piezoresistors from the accelerometer in figure 3. The central suspension beam (see figure 3) is preferably made much wider than this piezoresistor to assure that the bending occurs around the center of the device.

4. Experimental results

The accelerometers were designed to emulate a Wheatstone bridge, as was illustrated in figure 1. A half-bridge

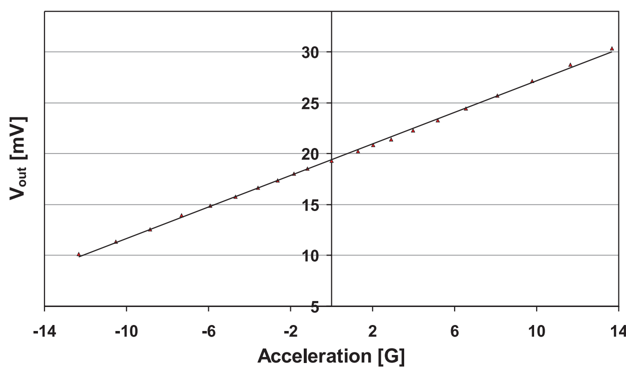

Figure 5. Accelerometer sensitivity measurements on rate table.

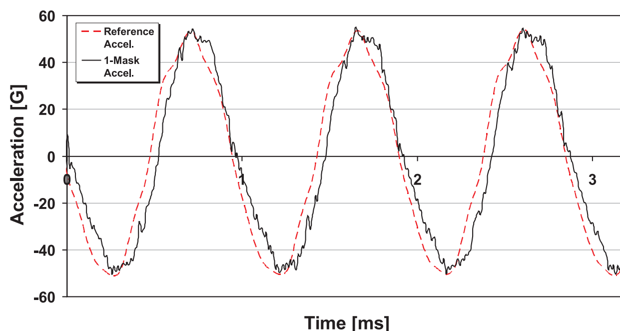

Figure 6. Time domain response at 1 kHz for a single-mask piezoresistive accelerometer and piezoelectric reference accelerometer.

configuration was used with both the piezoresistors and the reference resistors included on the chip. Applied acceleration causes bending of the centrally located suspension beam, and stretches one of the piezoresistors (increased resistance) and compresses the other (decreased resistance). This in turn leads to an unbalanced bridge and the output voltage is increased or decreased depending on the direction of the acceleration.

Diced SOI chips containing single-axis accelerometers were placed in dual in-line packages (DIP) and wire-bonded. For proof-of-concept, aluminum wires were bonded straight onto the silicon, without using metal bonding pads, making this truly a single-mask fabrication process. Adequate contacts can be provided in this manner due to the relatively high doping concentration in the p-type silicon. However, a contact resistance of about 50 Ω is measured in the bonded samples. In order to reduce this contact resistance and improve the ohmic contacts, a heavily doped surface layer and metal bonding pads should preferably be added to the process.

4.1. Sensitivity and time domain response

The packaged accelerometers were positioned 26 cm from the center of a rate table, which has a maximum angular velocity of 1300° s^{-1}. V_{in} was applied and V_{out} was measured through the rate table's slip rings. The velocity was increased in 100° s^{-1} increments from 400° s^{-1} to 1300° s^{-1}, corresponding to acceleration from approximately 1 G to 13 G. The same test was repeated with the accelerometer turned 180° and positioned 24 cm from the center of the rate table, inducing acceleration from approximately −1 G to −13 G.

Figure 5 shows linear output characteristics between −13 G and +13 G when V_{in} = 5 V was applied. The measured sensitivity was 0.77 mV G^{-1}. The voltage offset of 19 mV is due to fabrication imperfections that led to a slightly unbalanced Wheatstone bridge. Several approaches can be considered in order to eliminate this offset, including on-chip tuning resistors, off-chip shunt resistors, laser-trimming of the etched resistors, or using an external voltage-shifting circuit.

Next, a Dytran 3030A piezoelectric reference accelerometer was mounted in close proximity to the single-mask accelerometer to measure the time domain response, and the mounting platform was placed on a shaker. Figure 6 displays the output from both the reference accelerometer and the single-mask piezoresistive accelerometer at 1 kHz. Both outputs were ac coupled to eliminate the voltage offset. The sensitivity of the reference accelerometer was 10 mV G^{-1} and its maximum output during the excitation was 520 mV, yielding a maximum acceleration of 52 G. The single-mask piezoresistive accelerometer outputted approximately 40 mV for this acceleration, which is consistent with the sensitivity of 0.77 mV G^{-1}, previously obtained from figure 5.

While no significant phase shift is noted at 1 kHz, several different high-frequency components are sensed by the two accelerometers. This is the main reason for the mismatch between the curves in figure 6. The compliance of the package and the mounting bracket is believed to be the source of this discrepancy.

4.2. High-G testing

The accelerometers presented in this section were designed for impact testing applications with a maximum acceleration of 500 G. Figure 7(*a*) shows the time domain results from high-G testing, where an impact hammer was used to excite the piezoresistive accelerometer. The maximum measured impact was approximately 450 G. Note that the measured acceleration signal settles at about 25 G, which corresponds to the permanent offset of 19 mV from figure 5.

The high frequency oscillation of the signal in figure 7(*a*) is due to the undamped design of the accelerometer. From the fast Fourier transform (FFT) of the acceleration signal in figure 7(*b*), it can be seen that the frequency of this oscillation is approximately 7.6 kHz, which is consistent with the estimation of the natural frequency from section 2 (8.1 kHz). In future designs, a slight damping coefficient will be introduced by reducing the gap between the proof mass and the sidewalls of the bulk silicon in order to reduce this high-frequency oscillation.

4.3. Thermal characterization

A packaged accelerometer was placed inside a small thermal chamber together with a heater and a thermocouple. The chamber was then put on a rate table and the sensitivity and the voltage offset were measured at different temperatures during applied acceleration between 1 G and 16 G, as shown in figure 8.

The sensitivity of this accelerometer at room temperature was approximately 0.95 mV G^{-1} and the permanent voltage offset was 10.8 mV. As predicted from the discussion in

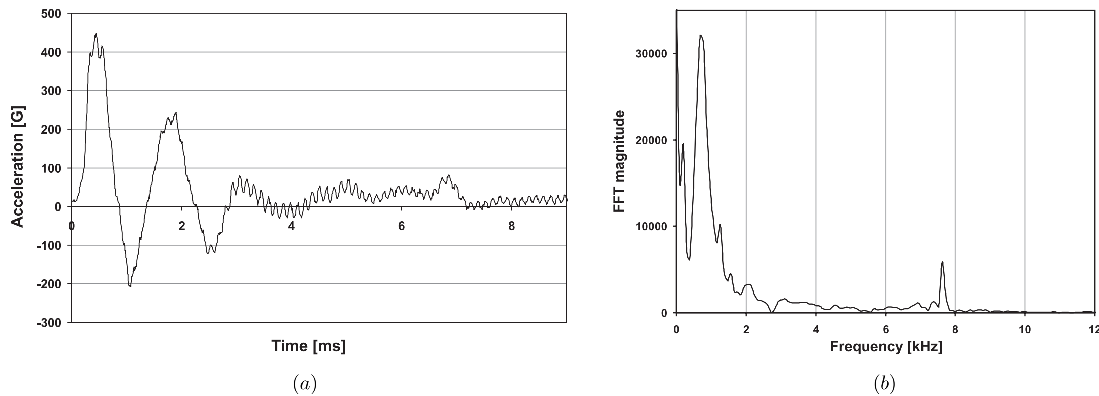

Figure 7. (*a*) Time and (*b*) frequency domain response of impact testing of the piezoresistive accelerometer.

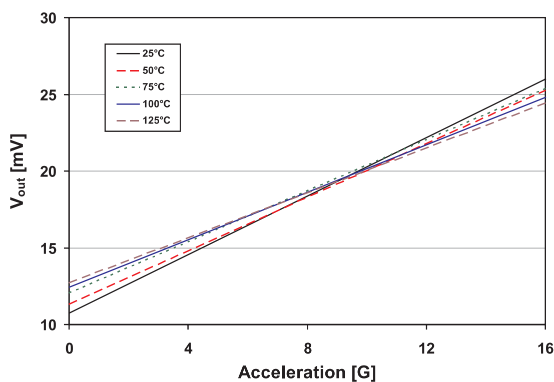

Figure 8. Thermal testing of the piezoresistive accelerometer.

Table 1. Offset voltage and sensitivity at elevated temperatures.

	25 °C	50 °C	75 °C	100 °C	125 °C
V_{out} (mV)	10.8	11.3	12.0	12.5	12.8
ΔV_{offset} (mV)	–	0.5	1.2	1.7	2.0
S (mV G^{-1})	0.95	0.87	0.83	0.77	0.73
$S/S_{25^\circ C}$	1	0.92	0.87	0.81	0.77
$P(N, T)$ [17]	1	0.92	0.86	0.80	0.75

section 2, the sensitivity was reduced at higher temperatures. However, while no significant change in voltage offset was expected due to the matching of the bridge resistors, a slight increase was observed in figure 8. This was likely due to fabrication imperfections and thermal stress in the material.

Table 1 summarizes the measured output voltage at zero acceleration and shows the obtained sensitivity at different temperatures. By dividing the sensitivity at an elevated temperature by the sensitivity at room temperature, the piezoresistive factor can be calculated (see section 2). As is shown in the table, the measured piezoresistive factors match the predicted values in [17].

The average temperature coefficient of sensitivity (TCS) is 0.3% °C^{-1} and the temperature coefficient of offset (TCO) is 20 mG °C^{-1}. While the TCS certainly needs to be compensated for, the TCO is not completely detrimental to the performance considering that the sensor is designed for acceleration between 1 G and 500 G. For example, if not properly compensated at 125 °C, the offset will show up as a false 2 G acceleration.

While the current testbed only allows for temperatures up to 125 °C, it has been demonstrated (for example [9, 12]) that isolation of piezoresistors using the buried oxide layer in SOI wafers is suitable for temperatures up to about 350 °C.

5. Conclusion

A single-mask fabrication process for piezoresistive accelerometers was presented. This process significantly reduces the number of required fabrication steps and also extends the operational temperature range, when compared to conventional piezoresistive accelerometers. Single-axis accelerometers were fabricated and characterized at high G-loads and different temperatures.

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