160 MILLI-OHM ELECTRICAL RESISTANCE THRU-WAFER INTERCONNECTS WITH 10:1 ASPECT RATIO

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Abstract

We present a novel approach for high-aspect ratio low resistance Thru-Wafer Interconnects for Double-Sided (TWIDS) fabrication of MicroElectroMechanical Systems (MEMS). The interconnects are formed by etching blind via holes in the handle substrate of an SOI (Silicon on Insulator) wafer, followed by filling the holes with copper, using sonic-assisted seedless copper electroplating process. This technique does not require additional conductive layer deposition, but utilizes a highly doped silicon device layer as a seed. The donut-shape gaps are etched around the copper filled vias to provide interconnects insulation. We introduced the fabrication process and characterized the performance of interconnects. Experimental analysis of an array of 22 interconnects demonstrated that the resistance values as low as 160 milli-Ohm can be achieved. Parasitic capacitance of interconnects is analytically calculated and the distortion of the MEMS resonator transduction spectrum is predicted using an equivalent circuit model. Signal amplitude and phase distortion due to the parasitic capacitance are estimated to be 1.15 dB and 5.96 deg, respectively, for the optimum 60 um diameter via with 35 um insulating gap. The method presented is compatible with an in-house folded MEMS fabrication process and may enable 3D folded TIMU (Timing Inertial Measurement Unit) structures with thru-wafer interconnects.

Key words

through wafer via, 3d interconnect, MEMS and IC integration, wafer level packaging, folded TIMU.

I. Introduction

High-aspect ratio thru-wafer interconnects technology has a wide spectrum of applications, ranging from multi-layer interconnects in integrated circuits to 3D packaging of MEMS sensors. The thru-wafer interconnects are typically intended to allow for co-integration of MicroElectroMechanical Systems and Integrated Circuits by utilizing the front and back side of a wafer.

The main challenges for thru-wafer interconnects are reduction of via size, low resistance and compatibility with standard semiconductor processing, [1].

The interest of this study is to develop a technology of Thru-Wafer Interconnects for Double-Sided (TWIDS) MEMS Fabrication Process.

This work focuses on interconnects for 3D folded Timing Inertial Measurement Unit (TIMU), Fig.1. In folded TIMU, thru-wafer interconnects provide a path for electrical signals from sensors on the device side of the wafer to ASIC (Application-Specific Integrated Circuit) components on the back side of the wafer, and allow at the same time for assembly of the integrated MEMS sensor cluster in a 3D configuration, or folding in a 3D shape [2].

Several approaches have been developed in literature for fabrication of thru-wafer interconnects, and the strategy for making the via can be divided into two categories. In the first category, thru-wafer interconnects are formed by the wafer material itself, e.g. a doped silicon via [3, 4, 5]. The method for forming the vertical via of the first category usually comprises the steps of patterning and etching
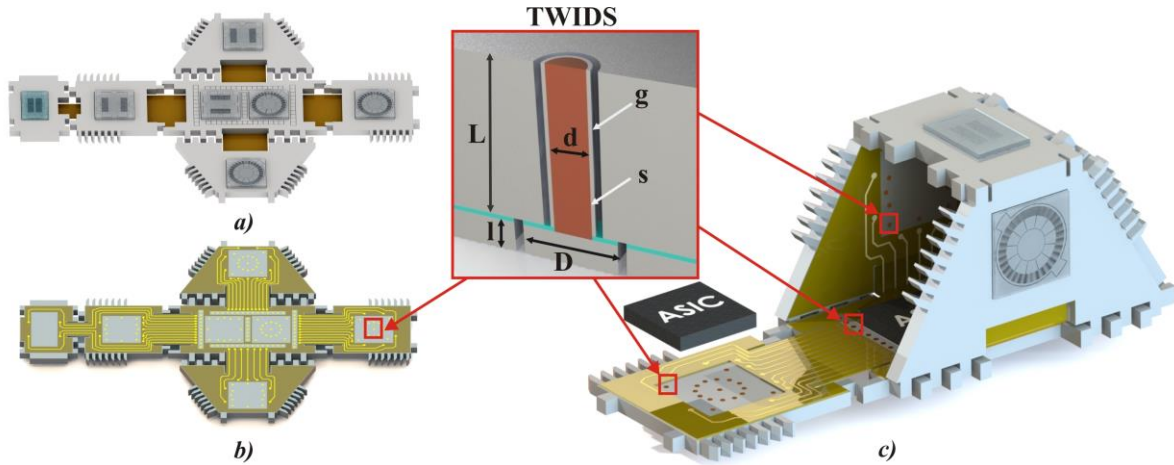
Fig. 1. MEMS Folded TIMU integrated with TWIDS process: a) unfolded structure (device side), b) unfolded structure (signal processing side), c) 3D assembled structure, showing device and signal processing sides.

through the silicon to isolate sections of a low resistivity silicon wafer; filling trenches with an insulating material, like glass or silicon dioxide; removing excess silicon; and depositing thin metal layer on the silicon parts.

In the second category, a vertical via hole is formed in the wafer using, for example, Bosch process [6], followed by an insulating layer and conductive layer deposition. A conductive layer, like highly doped polysilicon can be applied for electrical connection [7]. In other cases, a conductive layer provides a seed for subsequent metal electroplating process. Electroplating process is then used to fill the vertical vias with metal, e.g. copper [8] - [12]. In some cases, a conductive seed layer is not applied to the via wafer, then electroplating process utilizes a sacrificial wafer bonded to the thru hole via wafer [13], [14]. A sacrificial wafer is usually covered with a thin metal layer to serve for initiation of the plating process.

Thru-wafer interconnects of the first category, generally, have a relatively higher resistance as compared to thru-wafer interconnects of the second group due to the lower conductivity of silicon versus metal [3].

The technology for manufacturing thru-wafer interconnects of the second category has a number of limitations. Although thru-wafer vias of this kind reported earlier have shown satisfactory performance, fabrication of high aspect ratio (better than 10:1) and ultra-low resistance (lower than 200 milli-Ohm) interconnects remains problematic. The main challenge in the fabrication of metal, e.g. copper, electroplated interconnects is an uneven filling of the narrow and deep holes due to nonuniform deposition of a seed layer and insufficient wetting of the surface with copper electrolyte, leading to void formation. Most
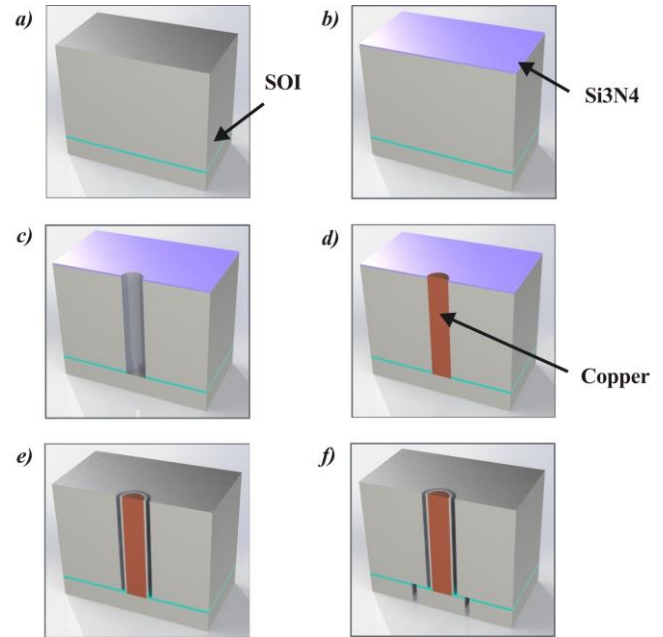

Fig. 2.TWIDS fabrication process steps: (a) SOI wafer, (b) LPCVD silicon nitride deposition, (c) defining thru-wafer holes, (d) seedless copper electroplating and lapping, (e) defining insulating gaps, (f) defining sensor features.

fabrication processes reported previously are complex, require rather sophisticated fabrication steps, including deposition of multiple layers or bonding a sacrificial wafer. High complexity of the fabrication process typically leads to a significantly decreased yield.

Objective of this research is to improve the fabrication process and the performance of interconnects. Our method addresses the challenges of interconnects assuring

continuity, high aspect ratio, electrical insulation, and void-free features.

II. Design and Fabrication

Our approach starts with deposition of a 1 um thick layer of low stress LPCVD silicon nitride on the surface of a 600 um SOI wafer, Fig. 2(a,b). We etch the 40, 60 and 80 um diameter blind via holes in the handle wafer, using Deep Reactive Ion Etching (DRIE). The etching is followed by removal of 5 um buried oxide layer, Fig.2(c). The holes are filled with copper using seedless copper electroplating that does not require additional conductive layer deposition, but utilizes a highly doped silicon device layer as a seed, Fig.2(d). The wafers are lapped to prepare for the next lithography step, and 30 um insulating gaps are etched around the copper filled vias, Fig.2(e). Finally, we define the sensor's features on the top side of the wafer, Fig. 2(f). To improve the quality of the copper filled TWIDS, different conditions for copper electroplating were explored. Fig. 3 illustrates cross-section of the TWIDS holes, electroplated with and without sonication. SEM analysis reveals that in a silent mode the electroplating solution could not penetrate into the high-aspect ratio via holes. As the result, via holes were not completely filled with copper, Fig. 3(a). We observed in our experiments that the sonication at frequency of 37kHz during the electroplating process significantly improved the filling, allowing for high aspect ratio voids-free interconnects, Fig. 3(b).
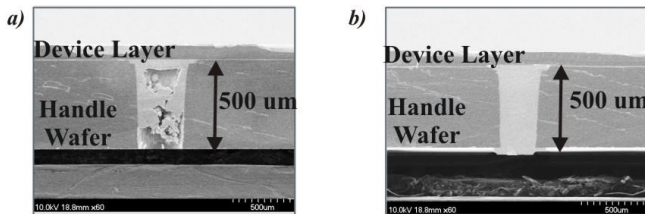

Fig. 3. Effect of using sonication in seedless copper electroplating process: (a) via hole electroplated at silent mode, (b) via hole electroplated in the presence of sonication.

III. Characterization and Discussion

We have successfully built an SOI inertial sensor with co-fabricated TWIDS, Fig. 4. The sensor was released using vapor HF process in order to remove a 5 um thick oxide layer under the moving structure. Probe tests revealed that the sensor contact pads were insulated. Experimental analysis of 22 interconnects of the diameters ranging from 40 to 80 microns showed resistance values as low as 160 milli-Ohm, Fig. 5.
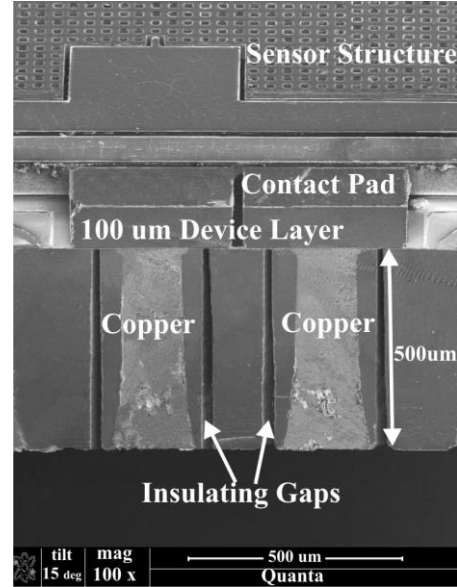

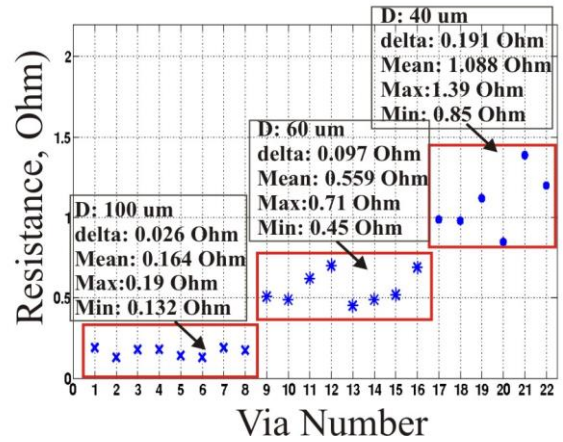Fig. 4. SEM picture of the MEMS inertial sensor with co-fabricated TWIDS.

Fig. 5. Resistance measurement for 22 interconnects, showing resistance less than 164 milli-Ohms for 100 um copper filled via

Parasitic capacitance may have a detrimental effect on the performance of MEMS inertial sensors with TWIDS, [15]. Implementation of an open-loop characterization technique for microsensor is a challenging task mainly because a relatively tiny motional current of the sensor is masked by parasitic feedthrough currents. There are a number of sources contributing to parasitic capacitance, including probe-to-probe capacitive feedthrough, pad-to-substrate capacitance, fringing field capacitance, and TWIDS capacitance, Fig. 6. TWIDS parasitic currents arise from thru-wafer silicon vias, which are surrounded by insulating
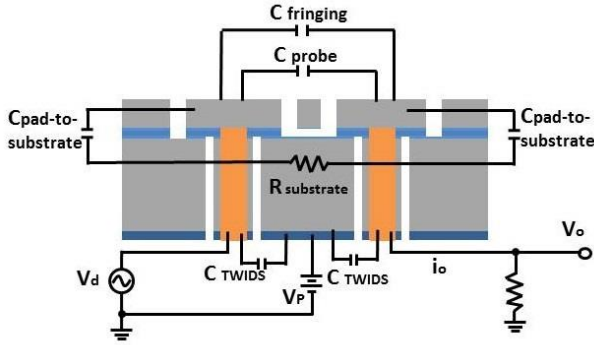
gaps and form capacitors with the silicon substrate.

Fig. 6. Schematic modelling of parasitics contributing to the distortion of the microsensor transduction spectrum. Electrostatic drive and sense with bias and excitation circuit configuration are included.
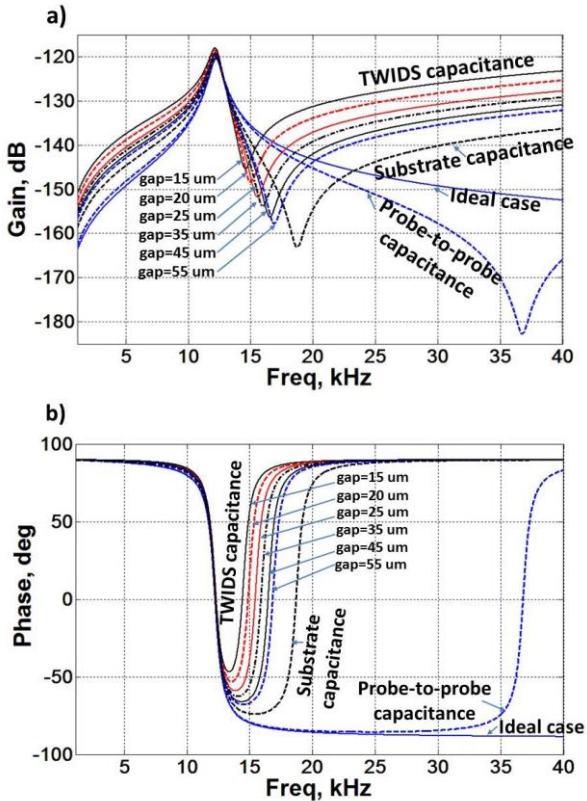

Fig.7. Transduction spectrum for an electrostatically driven microsensor, as predicted by its equivalent circuit model, for an ideal case, probe-to probe parasitic capacitance, substrate capacitance, and TWIDS capacitance: a) amplitude distortion, b) phase distortion.

Simulation in LTspice using the equivalent circuit elements for a microsensor, biased and excited as in Fig. 6, yields the transduction spectrum shown in Fig. 7. Based on

simulation, the transduction spectrum of a MEMS sensor was plotted under ideal conditions and with consideration of
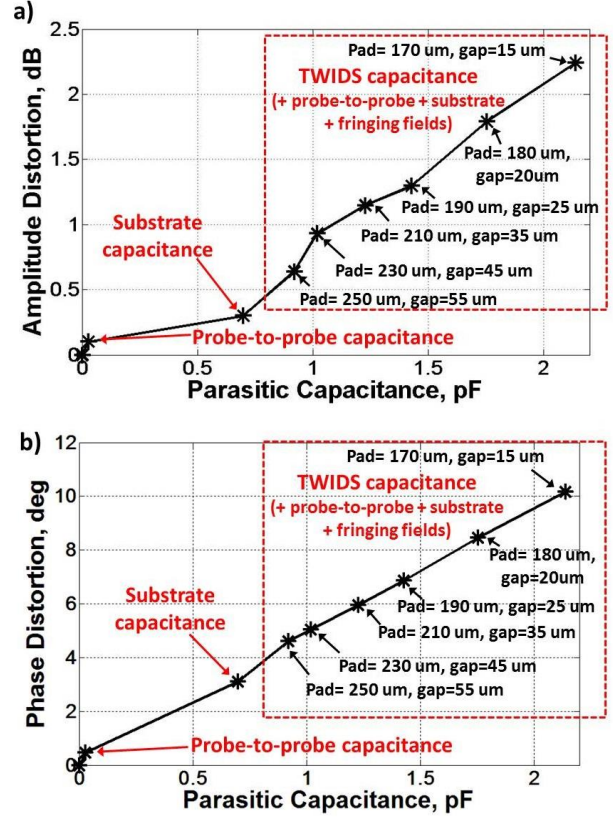

Fig.8. Signal distortion due to parasitic currents, as predicted by equivalent circuit model: a) amplitude distortion, b) phase distortion.

different sources contributing to parasitic feedthrough. In order to optimize parameters of the TWIDS process the thru-wafer interconnects parasitic capacitance was estimated for different widths of insulating gaps in the range of 15-55 um and the contact pads in the range of 170-250 um. Fig. 8 shows that the signal distortion due to via parasitic capacitance increases with decrease of an insulating gap and achieves 2.25 dB for amplitude and 10 deg for phase distortion in the case of 15 um insulating gap.

The design of the TWIDS involves a series of tradeoff decisions, such as insulating gap width, via hole diameter, silicon dioxide undercut area, and electrical contact pad size, Fig 1. The electrical contact pad size should not exceed 100-250 um, for most MEMS sensors applications. In order to minimize the size of the contact pad, the via hole, insulating gap, and the silicon dioxide undercut area should be minimized. However, these parameters are limited by the existing MEMS manufacturing tolerances. The via hole diameter and an insulating gap size are limited by the DRIE technology with aspect ratio of in the order of 20:1, in our implementation. Silicon dioxide undercut area

should be larger than 20×20 um to allow for successful release of sensors.

The optimum parameters for TWIDS are summarized in Table I. For the optimum electrical contact pad of 210 um with 60 um via hole and 35 um insulating gap, the TWIDS resistance across the vertical interconnects was experimentally demonstrated to be better than 710 milli-Ohms. The signal distortion due to parasitics was estimated analytically not to exceed 1.15 dB for amplitude and 5.96 deg for phase.

Table I. Optimum parameters for TWIDS

Parameter	Symbol	Value	Unit
Contact pad size	D	210	um
Handle wafer thickness	L	500	um
Device layer thickness	l	100	um
Via hole diameter	d	60	um
Insulating gap	g	35	um
Silicon dioxide undercut area	s	30	um
TWIDS resistance across vertical connection	R	< 0.71	Ohm
Signal amplitude distortion due to parasitic capacitance	ΔA	1.15	dB
Signal phase distortion due to parasitic capacitance	Δp	5.96	deg

IV. Conclusion

A TWIDS technology for fabrication of high density array of thru-wafer interconnects with resistance better than 710 milli-Ohm for 60 um diameter via and better than 164 milli-Ohm for 100 um diameter via has been presented.

TWIDS process is compatible with standard semiconductor processing, and suitable for co-integration with silicon sensors, such as MEMS accelerometers, gyroscopes and clocks. TWIDS were developed for 3D folded TIMU packaging to provide a path for electrical signals from sensors on the front side of the SOI wafer to electronic components on the back side of the wafer. The spectrum of applications of this technology is broad, TWIDS process is particularly appropriate for 3D packaging of MEMS devices.

Using the TWIDS technology, MEMS sensors with 210 um contact pads have been integrated on silicon wafer. Further reduction in the via size and aspect ratio can allow for minimizing the pad size and improving the inertial

sensors performance, as the sensor proof-mass area increases. However, reduction of the insulating gap size can lead to increase in parasitic capacitance. Thus, additional strategies should be implemented in order to minimize a detrimental effect of parasitic currents on the performance of MEMS sensors with TWIDS process, including grounding the handle substrate.

Acknowledgment

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