Thru-Wafer Interconnects for Double-Sided (TWIDS) Fabrication of MEMS

Alexandra Efimovskaya, Yu-Wei Lin, and Andrei M. Shkel
MicroSystems Laboratory, University of California, Irvine, CA 92697, USA
Email: {aefimovs, yuweil4, ashkel}@uci.edu

***Abstract*—This paper reports a new approach for fabrication of high-aspect ratio low resistance vertical interconnects, providing an electrical interface between the front-side and the back-side of the Silicon-on-Insulator (SOI) wafer. The method of Thru-Wafer Interconnects for Double-Sided (TWIDS) fabrication of MEMS is based on seedless copper electroplating, and allows for voids free features and high aspect ratio (copper diameter to wafer thickness ratio is 10:1). We introduced the fabrication sequence, implemented and characterized prototypes of a MEMS toroidal ring gyroscope with thru-wafer interconnects, thus illustrating the process feasibility. Furthermore, the critical issue of mechanical stability in air-gap interconnect structures under 15,000 g shock was investigated using 3D Finite Element Analysis (FEA) models. Our simulations revealed that a partial filling the gaps with Parylene C allows for 1.55x improvement in mechanical stability without a significant increase in via parasitic capacitance values.**

Introduction

The vertical thru-wafer electrical interconnects have recently gained a lot of interest in semiconductor industry due to compatibility with wafer-level packaging and multi-layer 3D packaging of MEMS and CMOS, as well as due to suitability of the approach for high-g shock environments. Packaging of MEMS sensors requires thru-wafer interconnects with high-aspect ratio, low resistivity, and low parasitic capacitance.

Several techniques for fabrication of vertical interconnects have been reported in literature, including single-crystal silicon vias, [1], polysilicon-filled vias, [2], and electroplated metal-filled vias, [3]. In most cases, silicon interconnects have higher resistance due to the lower conductivity of silicon versus metals. Electroplated metal-filled vias are typically formed by etching the vertical via holes, followed by deposition of an insulating layer, a seed layer, and metal electroplating.

Although thru-wafer metal vias reported earlier have shown a satisfactory performance, the realization of high aspect ratio interconnects (better than 10:1) remains a challenge. In high aspect-ratio via filling, void formation inside the via filling is a common problem. The main complication in the fabrication of metal, e.g. copper electroplated interconnects, is uneven filling of the narrow and deep holes due to non-uniform deposition of a seed layer. Insufficient wettability of via sidewalls and poor electrolyte chemistry are some of the other reasons behind the voids formation.

In this paper, we present a technology of thru-wafer interconnects, which is based on the bottom-up seedless copper electroplating and allows for void-free high-aspect ratio structures, Fig.1. Our method enables co-fabrication of MEMS SOI sensors with low-resistance copper thru-wafer interconnects.

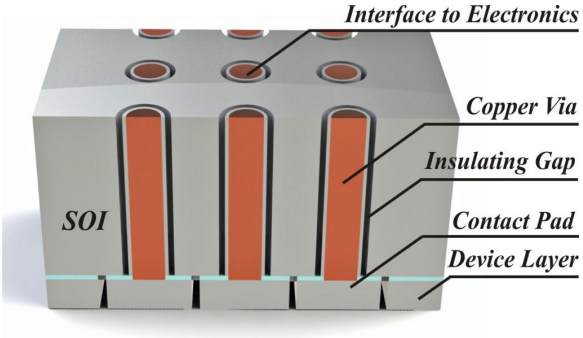

Fig. 1. High-density array of copper electroplated thru-wafer interconnects for MEMS double-sided process (TWIDS).

Process Flow

TWIDS fabrication process, [4], starts with a 600 μm thick SOI wafer with a thin 1 μm layer of low-stress silicon nitride on the handle side, Fig.2(a). The approach involves Deep Reactive Ion Etching (DRIE) of the blind thru-wafer holes, using a buried oxide layer as a stopper, Fig.2(b). Etching is followed by removal of oxide and filling the holes with copper, using a seedless electroplating method which does not require a conductive seed layer deposition and utilizes a highly doped silicon device layer to initiate the bottom-up plating process, Fig.2(c,d). Electroplating is performed in a custom-designed plating setup, consisted of a 4 inch copper electrode, an Elmasonic P 120H Ultrasonic unit, a DC power supply, and a bath with copper electrolyte (provided by TRANSENE, USA). The total electroplating time to fill the 500 μm deep vias is approximately 25 hr with a maximum current of 8 mA. To improve the quality of the filling, the ultrasound sonication in the range of 37 kHz is used during the first 10 min of the plating process. Silicon nitride acts as a barrier layer to prevent parasitic copper growing on the handle side of the wafer. Once plating is complete, the wafer is lapped and insulating gaps are DRIE etched around the copper-filled vias. Next, the SOI sensor's features are defined on the front side of the wafer, Fig.2(e,f).

Design and Fabrication

The TWIDS were designed for integration with SOI MEMS inertial sensors. 3D packaging of MEMS devices requires high

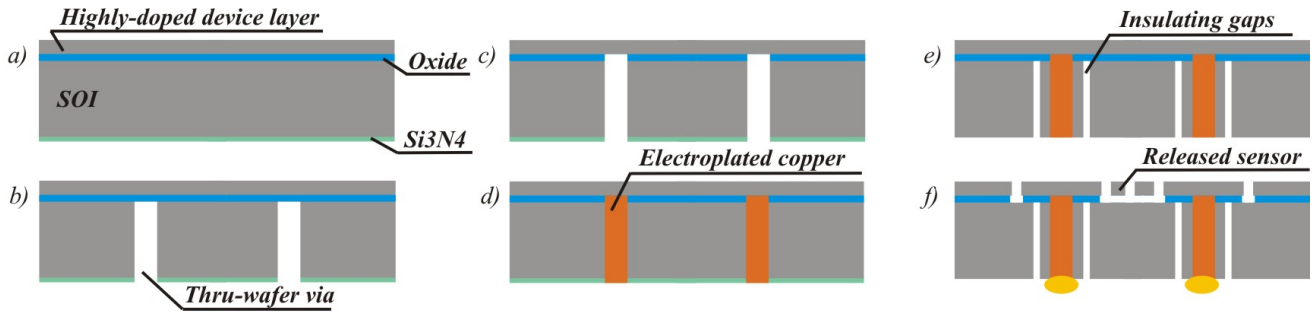

Fig. 2. TWIDS fabrication process: (a) SOI wafer, (b) thru-wafer via DRIE etch, (d) seedless copper electroplating and lapping, (e) defining insulating gaps, (f) sensor DRIE etch and release.

density array of interconnects with low resistance and low parasitic losses, assuring a low impedance path for electrical signals [5].

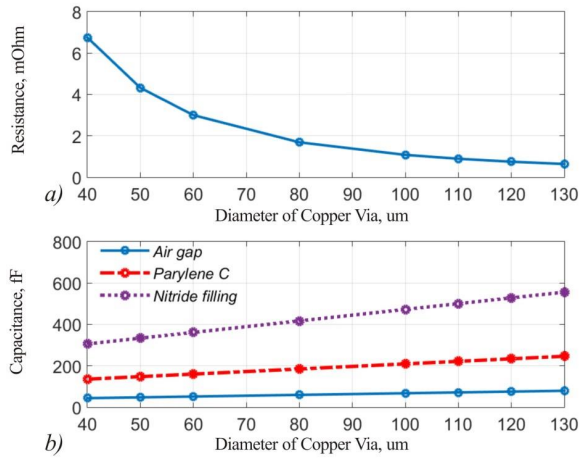

Fig. 3. Theoretical resistance and parasitic capacitance values for TWIDS as a function of diameter of copper-filled via

Theoretical resistance values for TWIDS are calculated as resistance of copper cylinder with a length of 500 μm and with a diameter in the range of 40 μm to 130 μm and parallel resistance of hollow Si cylinder with the wall thickness in the range of 20 μm to 35 μm. Fig. 3a) depicts the total theoretical resistance of TWIDS as a function of the copper via. The actual resistance of copper electroplated interconnects might be larger than bulk copper. An excess resistivity is associated with defects in electroplated film, [6]. The total resistance across the vertical interconnect also includes connected in series the resistance of a sensor contact pad. For the 380 μm contact pads with 100 μm diameter copper via the calculated theoretical value of the total resistance is 22 mΩ. The experimental value of the resistance across the 100 μm diameter copper via with a 380 μm contact pad was identified using a four-wire resistance measurement method, [4]. The measured value was less than 190 mΩ.

TWIDS parasitic capacitance arises primarily from copper vias, surrounded by insulating gaps and forming capacitors with the silicon substrate. Excess parasitic capacitance can lead to signal degradation, especially in high-frequency applications. Substrate coupling capacitance values were calculated as a function of the copper via diameter with a 35 μm donut-shaped air gap, Fig. 3b). The maximum value of 79 fF per interconnect was calculated for 130 μm diameter via. Isolation by filling the gaps with insulating material, such as silicon nitride or parylene, is also possible. The filling may improve the mechanical stability of interconnects, as shown in this paper. The filling of gaps, however, results in an increased parasitic capacitance of interconnects, Fig. 3b).

TWIDS with copper diameter in the range of 60 to 130 μm were fabricated, Fig.4. The interconnects can be utilized for sensors with contact pads as small as 200 μm by 200 μm. Further reduction of the via is limited by the DRIE etch aspect ratio, which is currently 16:1.

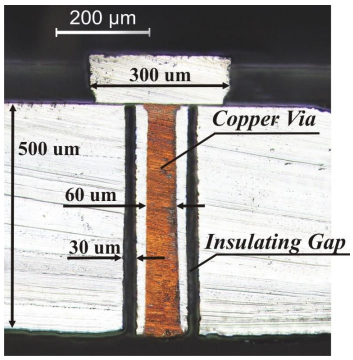

Fig. 4. Optical Microphotograph of the 60 μm diameter copper electroplated thru-wafer interconnect

Prototypes of a miniature 3.3 mm by 3.3 mm MEMS toroidal ring gyroscope, [7], with 100 μm diameter copper interconnects (copper diameter to wafer thickness up to 6:1) were fabricated using the TWIDS process, Fig.5. Scanning Electron Microscope (SEM) analysis was performed on the cross section of the electroplated thru-wafer vias and a continuous voids-free filling was demonstrated, Fig.6.

Experimental Results

Frequency response characterization of the sensors was performed using a custom-built test-bed, a Signatone probe station, and a set of probes for electrical connection of the

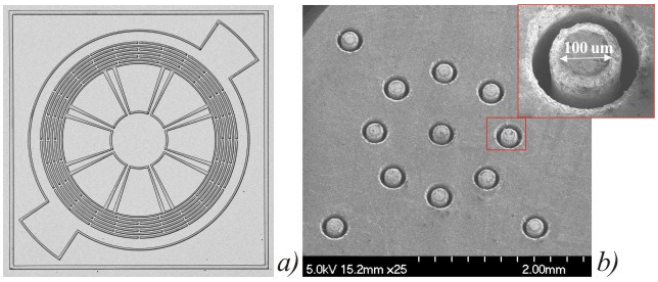

Fig. 5. A Prototype of MEMS toroidal ring gyroscope with co-fabricated TWIDS: a) front-side (device) view, b) back-side (interconnect) view.

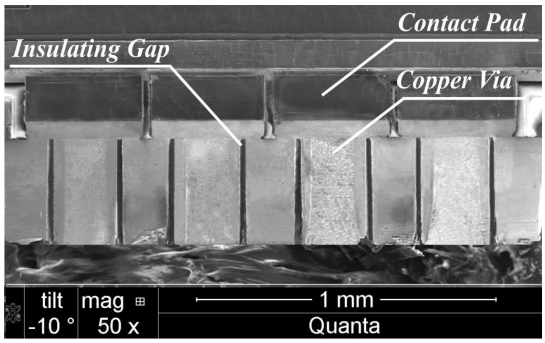

Fig. 6. SEM image of the MEMS inertial sensor with co-fabricated 100 μm diameter copper thru-wafer interconnects, showing voids-free features.

device contact pads to the electronic PCB board. The test-bed with a holder allows for testing the prototypes, using excitation/detection thru the top electrodes, when the sensor is "proof-mass-up", or thru the vertical interconnects, when the sensor is flipped, "proof-mass-down".

For the sensor excitation, a DC voltage of 24.8 V was applied to the proof mass and 1.5 V AC signal was applied to the drive electrodes. A series of experimental sweeps of the same sensor were obtained, using excitation/detection thru the top electrodes and thru the vertical interconnects, Fig.7.

The observed distortion of the frequency response is caused by the parasitic feedthrough currents, including TWIDS substrate coupling capacitance, pad-to-substrate capacitance, probe-to-probe capacitance, and PCB board parasitic capacitance. In order to identify the main source of the parasitics, we performed an analytical analysis of the transfer function of the overall system, including the parasitic effects, [8]. Shown in Fig.7, parasitic terms Cp (total capacitance in parallel with the sensor) and Rp (total parasitic resistance) were identified by examining the real and imaginary parts of a series of experimentally obtained responses.

The mean value of parasitic capacitance extracted from the frequency sweeps, obtained with excitation thru via was 1535 fF. The identified value of Rp was 2.2 MΩ. The mean value of parasitic capacitance extracted from the series of frequency sweeps, obtained with excitation thru top electrodes was 1407 fF. This suggests that TWIDS parasitic contribution into the response distortion was significantly lower that total parasitics of the setup.

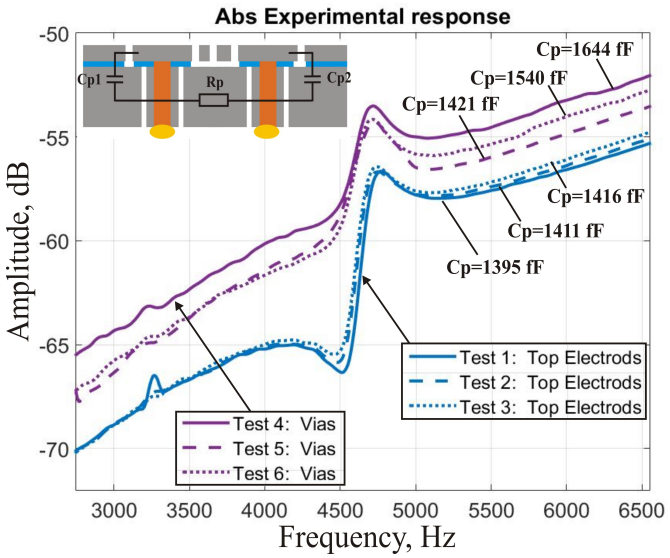

Fig. 7. Series of experimental sweeps of the sensor, obtained using excitation thru the top electrodes and thru vias.

To remove parasitic effects from the sensor output, the carrier demodulation technique was used, [8]. For that purpose, a high-frequency carrier signal of 100 kHz and amplitude of 0.5 V was applied to the structure. Frequency sweeps, obtained using excitation thru the top electrodes and thru vias, showed a good match, Fig.8.

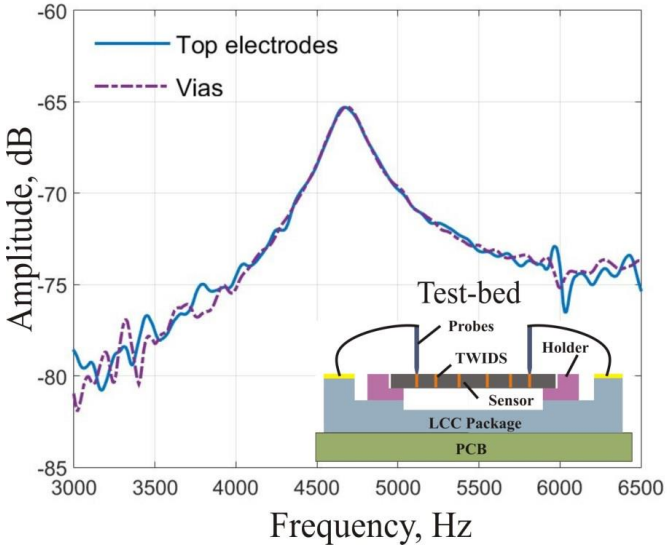

Fig. 8. Frequency sweeps, obtained using carrier demodulation technique, showed a good match between excitation/detection thru device-side and interconnect side.

Mechanical Stability

Limitations of the TWIDS technology are related to the mechanical stability of the structure, that can be compromised due to a high-density array of insulating air gaps. The wafer-level mechanical reliability during the post-processing is a

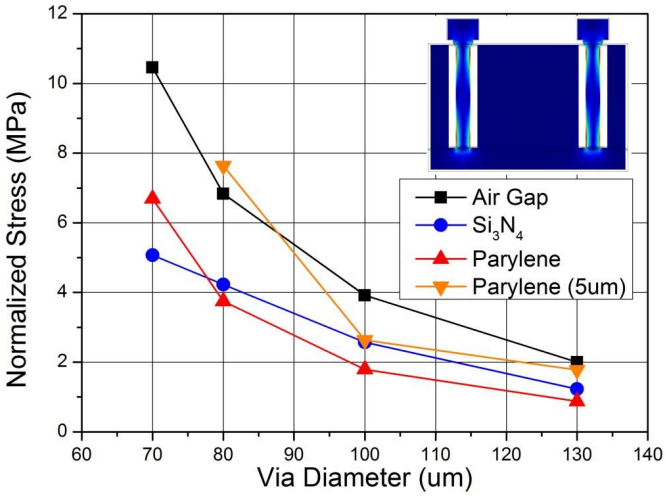

Fig. 9. Normalized principle stress in a die under 15000 g shock as a function of via diameter.

concern since once the integrity is lost, the wafers are prone to breakage [9]. The mechanical reliability of individual dies at the packaging assembly level, as well as during shock and vibrations is also an important issue.

The solution is sought in filling the insulating trenches by a dielectric material, such as Parylene C or silicon nitride. The choice of the filling material depends on vias applications and is a trade-off between the electrical, thermal, and mechanical properties of the interconnects. Parylene C, which has low relative permittivity of 3.1, is a good candidate for gaps filling. It is applied at room temperature and does not introduce any concerns for thermomechanical reliability of copper via. Moreover, Parylene deposition rate (about 5 μm/hr) is comparatively high, making it a suitable material for filling even large gaps (up to 35 μm).

Finite Element Method was used to analyze mechanical stability of via with the air gap and the insulator-filled gap. A model of a 3.3 mm by 3.3 mm silicon die with 600 μm thickness and 315 μm spacing between the vias was built. Stress distributions under shock with amplitude of 15000 g were calculated for via diameter in the range from 70 μm to 130 μm. We considered three cases: via with the 35 μm air gap, via with the gap fully filled with Parylene C or silicon nitride, and via with the gap partially filled with Parylene. Simulations showed that the maximum stresses are located at the point of via attachment to the contact pad and at the bonding interface, Fig. 9. Presented data is normalized to the values for solid wafers without via. Our study revealed that filling the gaps with parylene allows to reduce the stresses at the bonding interface by more than 2.2 times.

As discussed earlier, the filling of gaps results in an increased parasitic capacitance of interconnects, which may lead to significant signal degradation, especially in high frequency applications. In this case, an alternative approach where gaps are only partially filled with insulating material can be utilized. For example, partial filling of the gaps with Parylene C allows for 1.55x improvement in mechanical stability without a significant increase in via parasitic capacitance value (by less than 22 fF).

Conclusion

A novel approach for fabrication of high-aspect ratio low resistance copper thru-wafer interconnects was presented. The method is compatible with a standard SOI process and allows for voids free features and high aspect ratio (copper diameter to wafer thickness up to 10:1). We implemented and characterized prototypes of an SOI MEMS toroidal ring gyroscope with co-fabricated 6:1 aspect ratio thru-wafer interconnects. The series of experimental sweeps obtained with excitation thru top electrodes and thru interconnects, verified the feasibility of TWIDS technology. Furthermore, using FEA models, we investigated the mechanical stability of interconnects with air-gap and insulator-filled gap TWIDS under 15,000 g shock. Our simulations revealed that partial filling of the gaps with Parylene C allows for 1.55x improvement in mechanical stability without a significant increase in via parasitic capacitance value.

Due to the high aspect-ratio, low resistance and low parasitic capacitance, TWIDS technology may find a wide scope of applications, including 3D packaging of MEMS inertial sensors and RF MEMS.

Acknowledgment

This material is based upon work supported by DARPA grant N66001-13-1-4021 (Program Manager Dr. Robert Lutwak). Devices were designed, developed, and tested at UCI MycroSystems Laboratory. Authors would like to thank UCI INRF staff Jake Hes, and Mo Kebaili for their help and valuable suggestions on the fabrication aspects of the project.

References

[1] T. Bauer, *High Density Through Wafer Via Technology*, NSTINanotech, vol. 3, pp. 116119, (2007).

[2] E. M. Chow, V. Chandrasekaran, A. Partridge, T. Nishida, M. Sheplak, C. F. Quate, and T. W. Kenny, *Process compatible polysilicon-based electrical through-wafer interconnects in silicon substrates*, J. Microelectromechanical Syst., vol. 11, no. 6, pp. 631-640, (2002).

[3] N. T. Nguyen, E. Boellaard, N. P. Pham, V. G. Kutchoukov, G. Craciun, and P. M. Sarro, *Through-wafer copper electroplating for three-dimensional interconnects*, J. Micromechanics and Microengineering, vol. 12, no. 4, pp. 395-399, (2002).

[4] A. Efimovskaya and A. M. Shkel, *160 Milli-Ohm Electrical Resistance Thru-Wafer Interconnects With 10:1 Aspect Ratio*, Proc. IMAPS 47th Int. Symp. on Microelectronics, San Diego, USA, October 13-16, (2014).

[5] H. T. Soh, C. P. Yue, A. McCarthy, C. Ryu, T. H. Lee, S. S. Wong, and C. F. Quate, *Ultra-Low Resistance, Through-Wafer Via (TWV) Technology and Its Applications in Three Dimensional Structures on Silicon*, Jpn. J. Appl. Phys., vol. 38, no. Part 1, No. 4B, pp. 23932396, (1999).

[6] T. Moffat and D. Josell, *Superconformal Electrodeposition for 3D Interconnects*, Isr. J. Chemistry 2010, vol. 50, pp. 312-320, (2010).

[7] D. Senkal, E. Ng, V. Hong, Y.Yang, C. H. Ahn, T. W. Kenny, A. M. Shkel, *Parametric Drive of a Toroidal MEMS Rate Integrating Gyroscope Demonstrating $<$ 20 ppm Scale Factor Stability*, IEEE MEMS 2015, Estoril, Portugal, January 18-22, (2015).

[8] C. Acar, *Robust Micromachined Vibratory Gyroscopes*, PhD thesis, University of California at Irvine, (2004).

[9] A. Polyakov, M. Bartek, and J. Burghartz, *Mechanical Reliability of Silicon Wafers with Through-Wafer Vias for Wafer-Level Packaging*, Microelectronics Reliability, 42(9-11), pp. 1783-1788, (2002)