Double-Sided Process for MEMS SOI Sensors With Deep Vertical Thru-Wafer Interconnects

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***Abstract*— This paper reports an approach for co-fabrication of silicon-on-insulator (SOI) sensors with low-resistance vertical electrical interconnects in thick (up to 600 μm) wafers. The thru-wafer interconnects double-sided (TWIDS) process is based on bottom-up seedless copper electroplating, and allows for voids-free features and high aspect ratio (wafer thickness to copper diameter ratio of 10:1). This work describes the design trade-offs, process flow, and characterization of interconnects. TWIDS technology is compatible with a standard SOI micro-electro-mechanical systems (MEMS) fabrication process and is applicable for micro sensors, such as accelerometers, gyroscopes, resonators, and RF MEMS devices, as well as for the 3-D MEMS assemblies. As a demonstration of potential applications, miniature toroidal ring gyroscopes were fabricated using the TWIDS process. The experimental characterization showed that the low-resistance interconnects with low parasitic losses are suitable for integration with capacitive-detection sensors. In addition, the mechanical stability of the interconnects is discussed in this paper, and a method to enhance structural rigidity by means of filling the insulating gaps with Parylene C is demonstrated. [2017-0179]**

***Index Terms*— Thru-wafer via, 3-D interconnects, copper electroplating, MEMS and IC integration, wafer-level packaging, 3-D MEMS, micro-assembly.**

I. Introduction

THRU-WAFER electrical interconnects (TWI) have recently gained a lot of interest in semiconductor industry due to the continuous demands of the miniature MEMS devices for a faster signal transmission, better electrical performance, and compact packaging. The TWI technology is widely used in wafer-level packaging and multi-layer 3D integration of MEMS and CMOS.

The vertical interconnects find applications in 3D MEMS devices, for example in compact, multi-layer, vertically-stacked fused silica microsystems, [2], and folded MEMS Inertial Measurement Units (IMU), [3]. In folded IMU (Fig. 1), thru-wafer interconnects provide a path for electrical signals from sensors on the device side of the wafer to ASIC (Application-Specific Integrated Circuit) components on the handle side of the wafer, and allow at the same time for assembly of the integrated MEMS sensor cluster in a 3D configuration, when folded in a 3D shape.

For enhanced environmental robustness of 3D MEMS devices and assemblies, high aspect ratio interconnects have to be often formed in relatively thick wafers (up to 600 μm). This includes MEMS inertial sensors for harsh environments, tactile sensors, [4], and MEMS 3D assemblies, such as Folded MEMS IMU, where the substrate wafer forms a backbone for a 3D IMU structure. MEMS devices, like Folded IMU, require electrical feed-through interconnects with low resistivity and low parasitic losses, assuring a low impedance path for electrical signals.

Current approaches for fabrication of vertical interconnects can be divided into three general categories based on the material of the interconnect: single-crystal silicon vias, polysilicon-filled vias, and electroplated metal-filled vias.

Vias of the first category are usually formed by isolating sections of a low-resistivity silicon wafer. The isolation can be done by incorporating a trench filled with a dielectric material, [5]–[7], or by using a glass-in-silicon reflow process to create vias in glass wafers, [8]. Another approach involves anodic bonding of a pre-etched silicon wafer to a glass wafer, and then filling the silicon mold with glass, using a high-temperature reflow process.

The method of forming the polysilicon-filled vias usually comprises the steps of patterning and etching through the silicon wafer, deposition of an insulating material, like silicon dioxide, then filling via holes with doped polysilicon, [9], [10].

Fabrication of the electroplated metal-filled vias usually starts with forming of vertical via holes in a silicon wafer, using, for example, Bosch process, [11], or laser-ablation, [4]. This is followed by deposition of an insulation layer and a seed layer for the subsequent metal electroplating process. The via holes are then filled with metal, such as copper [4]–[13] or nickel [14], [15], using electroplating methods. In some cases, a conductive seed layer is not applied, instead a sacrificial wafer is bonded to the silicon wafer, [16], [17]. The sacrificial wafer is covered with a thin metal layer, for example copper or gold, to serve for initiation of the plating process.

Thru-wafer interconnects of the first category, single-crystal silicon vias, are usually formed by the wafer material itself, which significantly simplifies the fabrication process. However, silicon vias, generally, have a relatively higher resistance as compared to metal thru-wafer interconnects due

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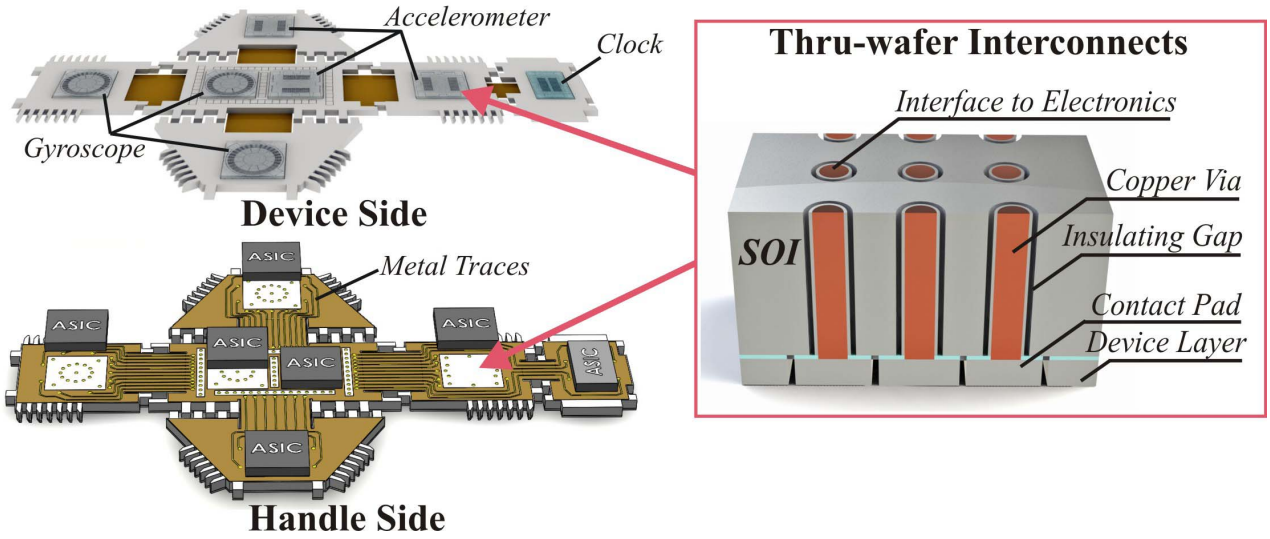

Fig. 1. Folded MEMS IMU. Thru-wafer interconnects enable electrical connection between the sensors on the device side of the wafer and electrical components on the handle side of the wafer.

to the lower conductivity of silicon versus metal. Polysilicon-filled vias are commonly preferred when high temperature processing steps follow the via fabrication. This technology is quite versatile but associated with a number of technical challenges, including uniformity of polysilicon filling in high aspect-ratio via holes and obtaining a high level of dopants during the deposition process, [18].

Metal thru-wafer interconnects deliver an advantage of high conductivity and are widely used in integrated circuits, MEMS packaging, and radio-frequency components. Vertical interconnects formed by copper electro-deposition is currently one of the key technologies for 3D integration of complex semiconductor devices. A number a methods have been recently proposed in literature for achieving void-free copper filling in high aspect ratio (>10:1) vias. This includes methods based on adding complex chemical additives into the plating bath, [19], periodic pulse reverse current, [20], [21], ultrasonic excitation, [22], and bottom-up filling process [23].

In this paper, we present a process for co-fabrication of MEMS sensors structures and copper-filled vertical interconnects in thick (up to 600 μm) Silicon-on-Insulator (SOI) wafers. The technology of metal thru-wafer interconnects is based on the bottom-up seedless copper electroplating and allows for void-free high-aspect ratio features. Seedless electroplating of metals, which is based on the direct plating on the surface of a silicon wafer, has been previously reported in literature. L. D. Vargas Llona et al. explored seedless electroplating of nickel on bare and patterned silicon wafers, [24]. T. Fujita et al. described a process for direct gold electroplating on silicon wafer [25]. A method of through-glass copper via using the glass reflow and seedless electroplating processes was proposed in [26]. In [26], copper electroplating was performed directly on the silicon wafer bonded on top of the glass wafer.

This paper reports a process where the single SOI wafer is used for co-fabrication of deep vertical copper interconnects and suspended micro structures (such as MEMS gyroscopes and accelerometers). Both sides of the wafer are processed, front side for patterning the device, back side for fabrication of seedless electroplated copper vias, where the highly doped Si device layer of the SOI wafer is used for direct deposition of copper. The double-sided process for thru-wafer interconnects co-fabricated with SOI sensors enables direct integration of MEMS sensors and 3D assemblies with ASIC or other types of heterogeneous integration.

II. Fabrication

The Thru-Wafer Interconnects Double-Sided (TWIDS) process, [27], allows for a high density array of vertical electrical feedthrough, providing an electrical interface between the front-side and the backside of the Silicon-on-Insulator (SOI) wafer.

TWIDS process flow, [28], starts with a 600 μm thick 4 inch diameter SOI wafer with a 100 μm thick highly-doped device layer (resistivity: 0.001 Ohm·cm), up to 500 μm thick handle layer (resistivity: 1-10 Ohm·cm), a 5 μm buried oxide layer in between, and a 1 μm thick layer of low stress LPCVD silicon nitride on the the handle side, Fig. 2(a). First, the wafer is spin-coated with a thick layer of AZ P4620 photoresist, the blind thru-wafer via holes are photo-lithographically defined, and the silicon nitride layer is etched using the STS MESC MULTIPLEX AOE System with the etch rate of 0.067 μm/minute, Fig. 2(b).

The blind thru-wafer via holes are then created, using a Deep Reactive Ion Etching (DRIE) of the handle wafer, while a buried oxide layer serves as an etch stopper, Fig. 2(b). The Plasma-Therm FDRIE DSE II Silicon Plasma Etching System is utilized for the deep DRIE etching. At this step, the etch rate for silicon is 5 μm/minute.

Etching is followed by removal of the buried oxide using a 20% HF solution, Fig. 2(c). Then the solvent cleaning is performed to remove the photoresist layer, left after the silicon dry etching step, followed by the RCA-1 aggressive cleaning of the wafer to remove the residual organic

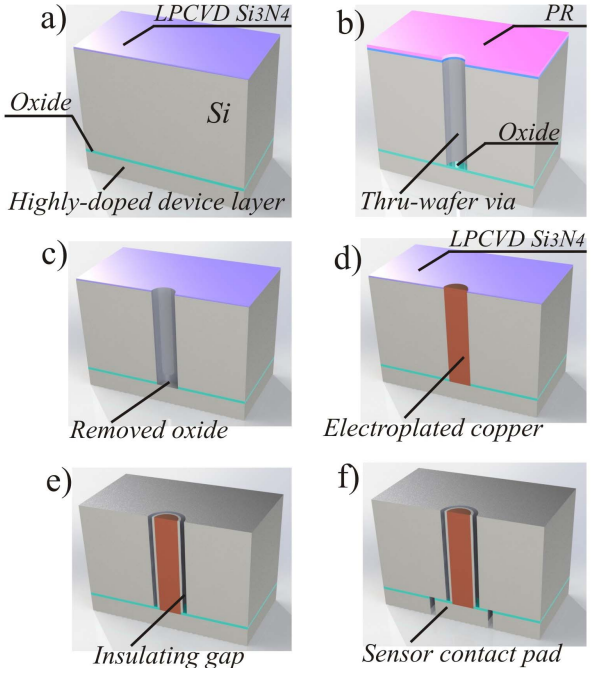

Fig. 2. TWIDS fabrication process: (a) SOI wafer, (b) thru-wafer via DRIE etch, (c) buried oxide removal, (d) seedless copper electroplating and lapping, (e) defining insulating gaps, (f) sensor DRIE etch and release.

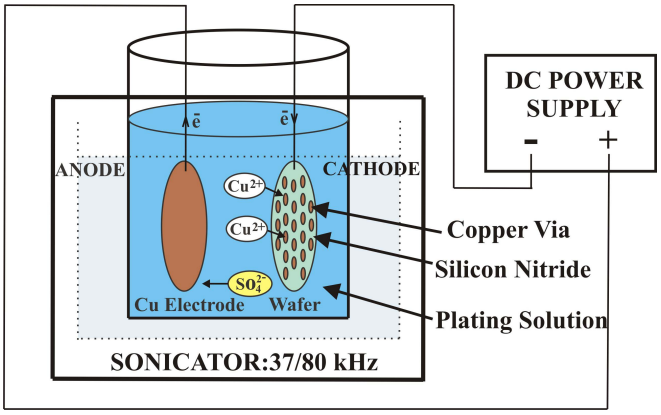

Fig. 3. Custom-designed plating setup includes a 4 inch copper electrode, an Elmasonic P 120H Ultrasonic unit, a DC power supply, and a bath with copper electrolyte.

material. Next, the via holes are filled with copper using a seedless electroplating method, which does not require a conductive seed layer deposition and utilizes a highly doped silicon device layer to initiate the bottom-up plating process, Fig. 2(d).

Electroplating is performed in a custom-designed plating setup, Fig. 3, which includes a 4 inch copper electrode, an Elmasonic P 120H Ultrasonic unit, a DC power supply, and a bath with copper electrolyte. Copper electrolyte is a copper plating acid type solution (provided by TRANSENE, USA), which consists of copper sulfate, hydrochloric acid, and sulfuric acid. Addition agents in a bath include a brightener and a leveler.

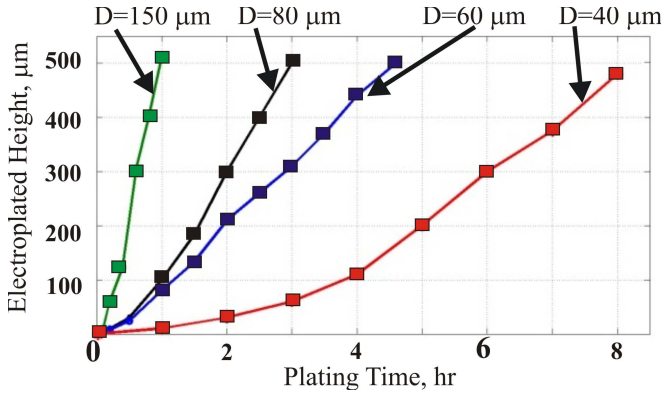

Fig. 4. Total electroplating time to fill the 500 μm deep vias depends on the via diameter and varies in the range from 1 hr to 8 hr.

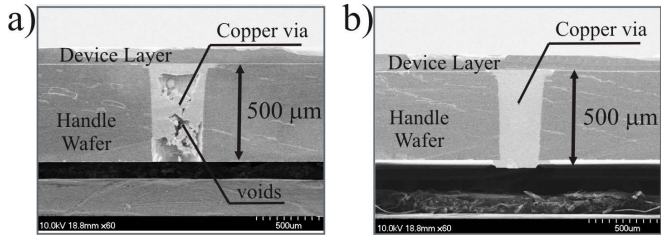

Fig. 5. (a) Vias electroplated in a silent mode, (b) vias electroplated in the presence of sonication.

Electroplating was performed at room temperature with the current density of 5 mA/cm^2. The total electroplating time to fill the 500 μm deep vias depends on the via diameter and varies in the range from 1 hr for 150 μm diameter vias to 8 hrs for 40 μm diameter vias, Fig. 4. LPCVD silicon nitride deposited on the handle side of the wafer acts as a barrier layer to prevent parasitic copper growth and to reduce the plating time.

To further improve quality of the filling, different conditions for copper electroplating were explored. Fig. 5 illustrates the cross-section of the vias electroplated with and without sonication. SEM analysis revealed that in a silent mode the electroplating solution could not penetrate into the high-aspect ratio via holes. As the result, interconnects were not completely filled with copper, Fig. 5(a). We observed in our experiments that sonication in the range of 37 kHz during the first 10 min of the plating process significantly improved the filling, allowing for high aspect ratio voids-free interconnects, Fig. 5(b).

Once plating is complete, the back side of the copper-electroplated wafer is lapped to prepare for the following photo-lithography step. Lapping is performed using a 12" MultiPrep Polishing System (available from Allied High Tech Inc.) and a set of diamond lapping films with a size of diamond particles 30, 15, 6, 3, and 1 μm. At the end of the polishing process, a diamond suspension with 0.25 μm particles is used for creating an optically smooth surface finish. Alternatively, a chemical mechanical polishing (CMP) can be utilized to polish the wafer surface.

Next, the wafer is spin-coated with a thick layer of AZ P4620 photoresist, the insulating gaps are photo-lithographically defined around the copper-filled vias and are

DRIE etched, Fig. 2(e). The SOI sensor's features are then defined on the front side of the wafer, Fig. 2(f). Sensor definition involves spin-coating the wafer with a thin layer of Shipley 1827 photoresist, photo-lithography to create the etch mask, followed by etching the 100 μm silicon device layer using the STS DRIE System. Photoresist stripping by solvent cleaning completes the fabrication process.

The suspended MEMS structures are then released using a stiction-free vapor HF process to remove the buried oxide layer under the device suspension and proof mass. The released proof-mass is left suspended above the substrate wafer and it is connected to the stationary anchors by means of the flexible suspension. Similar to the standard SOI fabrication process, the time of the HF etching step has to be controlled. If the proof-mass of the sensor is formed by the uniform membrane, the proof-mass has to be perforated with release holes in order to increase the release rate of the suspended structure. In case of the ring type sensors, such as a Toroidal Ring Gyroscope (TRG), [30], the proof-mass is formed by the series of thin rings. For example, for a TRG with 10 μm thick rings and 10 μm spacing between the rings, the etch rate of the buried oxide layer under the suspension is >14 times higher than the etch rate of the buried oxide layer under the anchors with vias. In addition, the vias side of the wafer is partially protected with the dicing tape (Semiconductor Equipment Corp., USA) and is placed in a close contact with the HF chamber electrostatic chuck to avoid the direct contact with HF vapor.

Depending on the application, the conductive vias can be mechanically reinforced by means of filling the insulating gaps with polymer or other dielectric materials.

III. Electrical Characterization

The key features of the vertical interconnects for 3D MEMS structures are the small footprint, high conductivity, and low parasitic losses, ensuring good electrical performance.

Theoretical resistance values for TWIDS are calculated as resistance of copper cylinder with a length of 500 μm and with a diameter in the range from 40 μm to 130 μm and parallel resistance of hollow Si cylinder with the wall thickness in the range from 20 μm to 35 μm. In our calculations, we assumed Cu resistivity of 1.7 μOhm·cm and Si handle wafer resistivity of 10 Ohm·cm. Fig. 6(a) depicts the total theoretical resistance of TWIDS as a function of the copper via diameter. The actual resistance of copper electroplated interconnects might be larger than bulk copper. An excess resistivity is associated with defects in electroplated film, [29]. The total resistance across the vertical interconnect also includes, connected in series, the resistance of a sensor contact pad. For the 380 μm contact pads with 100 μm diameter copper via the calculated theoretical value of the total resistance is 22.1 mΩ. For the 300 μm contact pads with 60 μm diameter copper via the calculated theoretical value of the total resistance is 29.6 mΩ.

TWIDS parasitic capacitance arises primarily from copper vias, surrounded by insulating gaps and forming capacitors with the silicon substrate. Excess parasitic capacitance can lead to signal degradation, especially in high-frequency applications. Substrate coupling capacitance values were calculated as a function of the copper via diameter with a 35 μm donut-shaped gap, Fig. 6(b). For the air gap, the maximum value of 68 fF per interconnect was calculated for 100 μm diameter via. Isolation by filling the gaps with insulating material, such as silicon nitride or parylene, is also possible. The filling may improve the mechanical stability of interconnects, [1]. The filling of gaps, however, results in an increased parasitic capacitance of interconnects, Fig. 6(b).

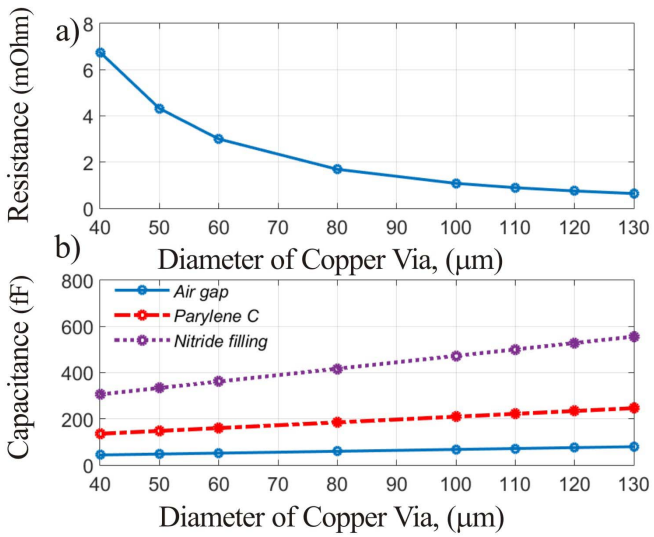

Fig. 6. (a) Theoretical resistance and (b) theoretical parasitic capacitance values for TWIDS as a function of copper via diameter.

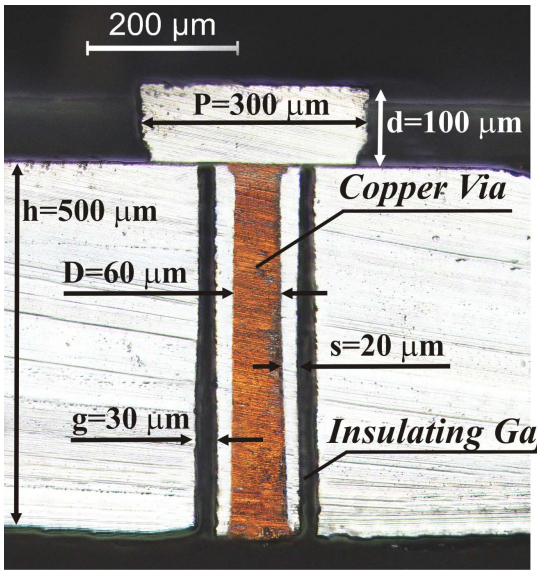

Fig. 7. Optical Micro-photograph of the 60 μm diameter copper electroplated thru-wafer interconnect.

Using TWIDS process, vertical interconnects with copper diameter of 60 and 100 μm were fabricated, Fig. 7. Dimensions of the fabricated interconnects are summarized in Table I.

Resistance across the thru-wafer interconnects was measured using a four point probe method, which allows for eliminating the effect of contact resistance between a probe

TABLE I
DIMENSIONS OF THE FABRICATED INTERCONNECTS

	60 μm Via	100 μm Via
Cu diameter, D	60 μm	100 μm
Handle wafer thickness, h	500 μm	500 μm
Device layer thickness, d	100 μm	100 μm
Si wall thickness, s	20 μm	35 μm
Insulating gap width, g	30 μm	35 μm
Contact pad, P	300 μm	380 μm

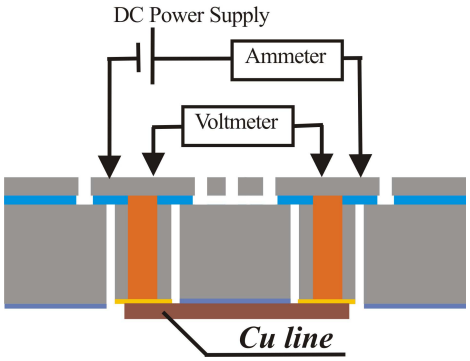

Fig. 8. Four-point resistance measurement setup.

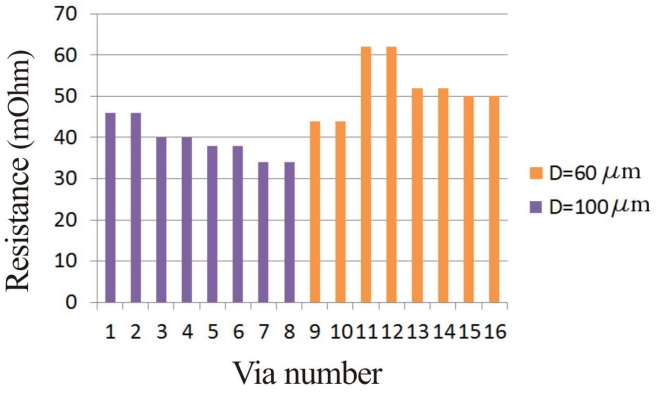

Fig. 9. Measured resistance of the 60 μm diameter and 100 μm diameter copper electroplated thru-wafer interconnects.

and an electrical contact pad, and allows for eliminating an error induced by the resistance of wires.

A schematic drawing of a measuring setup is shown in Fig. 8. In our measurement, a chain of two interconnects was connected on the backside of the wafer using a Cu line formed by a highly-conductive copper tape. The resistance value of individual via was calculated as:

$$R_{TWIDS} = 0.5(R_{meas} - R_{Cu-line}), \quad (1)$$

where R_{meas} is the measured resistance value of a pair of interconnects, $R_{Cu-line}$ is the resistance of the Cu backside line, which varied in the range from 35 to 68 mOhm for different pairs of interconnects. The results of measurement of 8 via chains are shown in Fig. 9.

The measured resistance of 100 μm via ranged from 34 to 46 mOhm, with an average value of 39.5 mOhm, and a

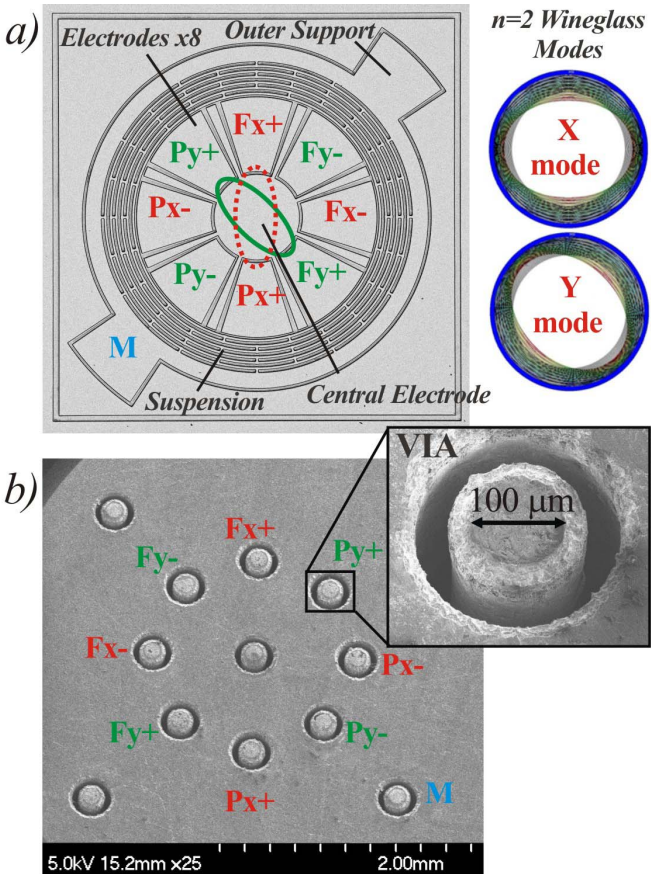

Fig. 10. Prototype of MEMS Toroidal Ring Gyroscope with co-fabricated TWIDS: a) front-side (device) view, b) back-side (interconnect) view.

standard deviation of 4.3 mOhm. The measured resistance of 60 μm via ranged from 44 to 62 mOhm, with an average value of 52 mOhm, and a standard deviation of 6.5 mOhm. The average value of the resistance is higher than the analytically predicted value. This error is mainly due to inaccuracy in measurement of the Cu line resistance and an additional contact resistance between the backside Cu line and a via.

IV. SOI MEMS GYROSCOPE INTEGRATED WITH TWIDS

Thru-wafer interconnects fabricated using TWIDS process can be utilized for SOI sensors with contact pads as small as 200 μm by 200 μm. Further reduction of the via is limited by the DRIE etch aspect ratio, which is currently 16:1 in our process.

A. Sensor Design

Prototypes of a miniature 3.3 mm by 3.3 mm MEMS Toroidal Ring Gyroscope, [30], with 100 μm diameter copper interconnects (wafer thickness to copper diameter up to 6:1) were fabricated using the TWIDS process, Fig. 2. Fig. 10 shows the front and the backside view of the fabricated sensor.

Toroidal Ring Gyroscope (TRG) is comprised of an inner electrode assembly, an outer support, and a concentric-ring suspension, Fig. 10 (a). The suspension is formed by the

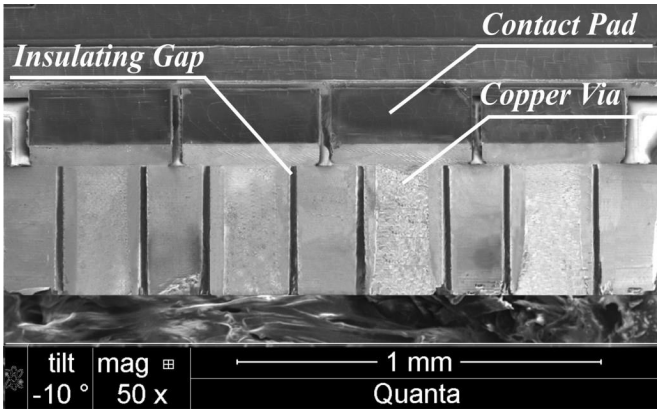

Fig. 11. Cross-section of several vias, uniformly filled with copper.

10 μm thick concentric rings with 10 μm spacing between the rings. The mechanical element of the gyroscope is a planar resonating structure which has degenerate pairs of in-plane wineglass vibration modes. The gyroscope is designed to operate in the n=2 wineglass mode. The inner electrode assembly consists of 8 radial electrodes that are used as a forcer and as a pick-off, for each of the modes. The central star-shaped electrode acts as a shield by sinking parasitic currents between discrete electrodes.

Enabled by the TWIDS process, one thru-wafer via is connected to the center electrode and one per each electrode in the inner electrodes assembly; two vias are connected to the outer anchor, and two are connected to the frame surrounding the sensor to be used for substrate grounding, Fig. 10 (b). Thru-wafer interconnects allow for the electrical connection between the front side and the back side of the sensor die.

Cu plating uniformity is an important issue since even closely placed vias may show different Cu plating rate, [31]. To improve the plating uniformity, Cu was over plated during the bottom-up electroplating step, Fig. 2(d). Once all the vias were filled, the wafer polishing was performed to remove the redundant Cu at the wafer backside. The cross-section of several vias on the same die, uniformly filled with copper, is shown in Fig. 11. In average for 8 sensor dies from the same wafer, 80% of interconnects across one die were completely filled with metal.

B. Experimental Results

Frequency response characterization of the sensors was performed using a custom-built test-bed, a Signatone probe station, and a set of probes for electrical connection of the device contact pads to the front-end PCB. The test-bed with a holder allows for testing the prototypes, using excitation/detection thru the top electrodes, when the sensor is "proof-mass-up", or thru the vertical interconnects, when the sensor is flipped, "proof-mass-down", Fig. 12.

The sensor was excited to oscillate in the first wineglass mode in n=2 pair, indicated as X mode in Fig. 10 (a). For the sensor excitation, one probe was used to apply a DC voltage of 24.8 V to the proof-mass (electrode M in Fig. 10(a), (b)) and one probe was used to apply a 1.5 V AC signal to one

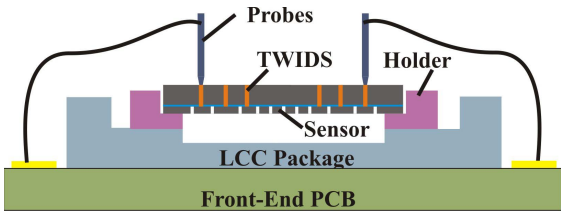

Fig. 12. Custom-built test-bed with a holder for testing sensors, using excitation/detection thru top electrodes or thru vertical interconnects.

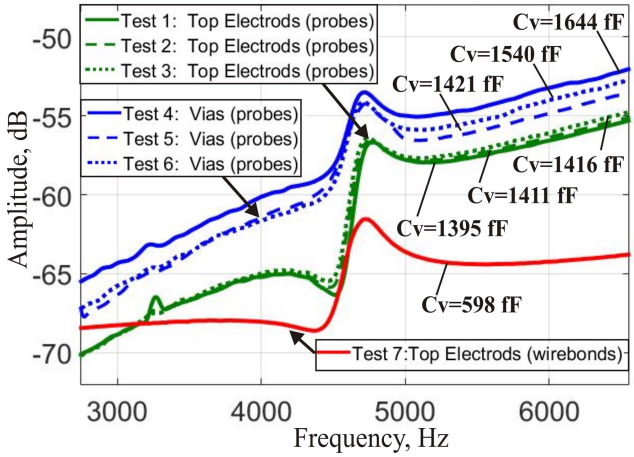

Fig. 13. Series of experimental sweeps of the sensor, obtained using excitation thru the top electrodes and thru vias.

out of two differential drive electrodes (electrodes Fx+ and Fx− in Fig. 10(a), (b)). Another probe was connected to one out of two differential pick-off electrodes (Px+ and Px− in Fig. 10(a), (b)). A series of experimental sweeps of the same sensor were obtained, using excitation/detection with probes connected to the top electrodes and to the vertical interconnects, Fig.13.

The observed distortion of the frequency response is caused by the parasitic feedthrough currents, including TWIDS to substrate coupling capacitance, pad-to-substrate capacitance, probe-to-probe capacitance, and PCB parasitic capacitance. In order to identify the main source of the parasitics, we performed an analytical analysis of the transfer function of the overall system, including the parasitic effects, [32]. Parasitic capacitance and resistance values were then extracted using a series of experimentally obtained responses, Fig. 13.

The transfer function of the electro-mechanical resonator system can be represented as:

$$\frac{V_0}{V_{in}} = K\frac{\chi_1\chi_2 s}{ms^2 + cs + k}, \tag{2}$$

where K is the transimpedance amplifier gain, c and k are the damping and stiffness coefficients, correspondingly, and χ_1 and χ_2 are the coefficient for conversion from the input signal to mechanical force and for the mechanical displacement to motion induced current, correspondingly.

In the case of sensor excitation/detection using top electrodes (Fig. 14), we included the parasitic feed-through current which runs through the driving contact pad, then through

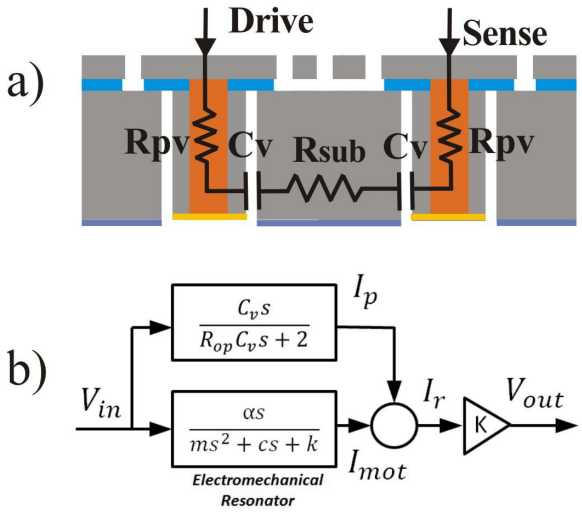

Fig. 14. (a) Schematic of a system with excitation/detection using top electrodes, (b) transfer function model of the system including parasitic feed-trough current.

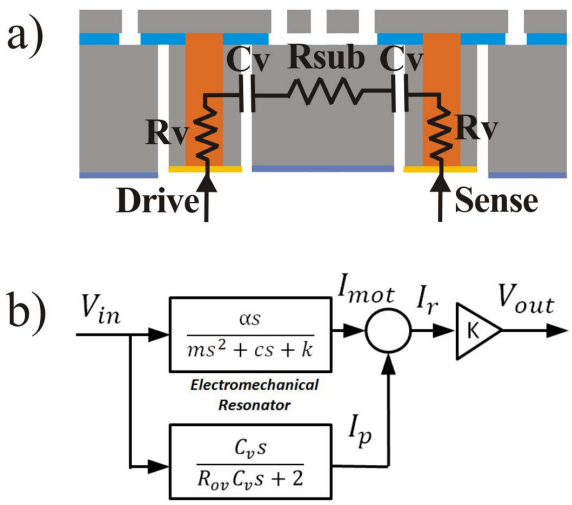

Fig. 15. (a) Schematic of a system with excitation/detection using vias, (b) transfer function model of the system including parasitic feed-trough current.

the first via, parasitic capacitance of the first insulating gap, through the substrate, then through parasitic capacitance of the second insulating gap, through the second via, and, finally, through the sensing contact pad:

$$\begin{aligned}
\frac{V_0}{V_{in}} &= K\frac{\chi_1\chi_2 s}{ms^2+cs+k} + K\frac{C_p s}{R_{op}C_p s+1} \\
&= K\frac{\chi_1\chi_2 s}{ms^2+cs+k} + K\frac{C_v s}{R_{op}C_v s+2}, \\
R_{op} &= R_{pv1} + R_{sub} + R_{pv2}, \\
R_{pv1} &= R_{pad1} + R_{Cu1} + R_{Si1}, \\
R_{pv2} &= R_{pad2} + R_{Cu2} + R_{Si2}, \qquad (3)
\end{aligned}$$

where C_v is the parasitic capacitance of via, R_{pad1} and R_{pad2} are the resistance values of the driving and sensing contact pads, R_{Cu1} and R_{Cu2} are the resistance values of the first and second copper vias, R_{Si1} and R_{Si2} are the resistance values of the silicon surrounding the first and second vias, R_{sub} is the resistance of the substrate.

In the case of sensor excitation/detection using vias (Fig. 15), we included the parasitic feed-through current which runs through the resistance and parasitic capacitance at the driving port via, through the substrate, then through the resistance and parasitic capacitance at the sensing port via:

$$\begin{aligned}
\frac{V_0}{V_{in}} &= K\frac{\chi_1\chi_2 s}{ms^2+cs+k} + K\frac{C_v s}{R_{ov}C_v s+2}, \\
R_{ov} &= R_{v1} + R_{sub} + R_{v2}, \\
R_{v1} &= R_{Cu1} + R_{Si1}, \\
R_{v2} &= R_{Cu2} + R_{Si2}. \qquad (4)
\end{aligned}$$

The real and imaginary parts of the frequency response (3) were then analyzed:

$$Re(n) = \frac{R_{op}C_v^2\omega_n^2}{(R_{op}C_v\omega_n)^2+4}, \qquad (5)$$

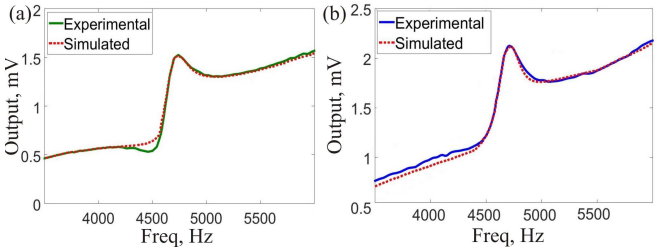

Fig. 16. Experimental freq. response curves obtained using electrical connection through (a) top electrodes, (b) vias are fitted to the simulated response curves with the analytically identified system parameters.

where $Re(n)$ is the offset in the real part of the experimentally extracted frequency response at frequency ω_n, away from the resonance point, and

$$Im(r) = \frac{2C_v\omega_r}{(R_{op}C_v\omega_r)^2+4}, \qquad (6)$$

where Im_r is the imaginary part of the experimentally extracted frequency response at resonant frequency ω_r.

Equations (5) and (6) were solved simultaneously to identify parasitic terms C_v (parasitic capacitance) and R_{op} (total resistance) for the system in Fig. 14. Following the described procedure, parasitic terms C_v and R_{ov} for the system in Fig. 15 were also identified using equation (4) and by examining the real and imaginary parts of experimentally obtained responses.

Fig. 16 shows the experimentally acquired frequency response curves fitted to the simulated response curves with the analytically identified system parameters. The close match between the experimental and simulated curves verifies the accuracy of the system parameters and parasitic terms estimation.

Calculated values of parasitic capacitance are shown in Fig. 13, including capacitance C_v for frequency sweeps obtained using electrical connection through top electrodes and parasitic capacitance C_v for frequency sweeps obtained using electrical connection through vias. The mean value of

parasitic capacitance extracted from the frequency sweeps, obtained with excitation thru via was 1535 fF. The mean value of parasitic capacitance extracted from the series of frequency sweeps, obtained with excitation thru top electrodes was 1407 fF.

The experimentally identified values of the parasitic capacitance are higher than the calculated theoretical values, Fig. 6(b). It has been hypothesized that the probe-to-probe capacitance is one of the major factors contributing into the parasitic feedthrough current. Including the probe-to-probe capacitance in parallel with the sensor results in a following transfer function of the system in Fig. 14:

$$\frac{V_0}{V_{in}} = K\frac{\chi_1\chi_2 s}{ms^2 + cs + k} + K\frac{C_v s}{R_{op}C_v s + 2} + C_{probe}s, \quad (7)$$

where C_{probe} is the probe-to-probe parasitic capacitance.

To eliminate the effect of the probe-to-probe capacitance, the sensor's top contact pads were wirebonded to the gold pads of the LCC (Leadless Chip Carrier) package. The value of parasitic capacitance $C_v = 598$ fF was then extracted using the equation (3) and the experimentally obtained frequency sweep, Fig. 12, Test 7. This result suggests that TWIDS parasitic contribution into the response distortion was significantly lower than the total parasitics of the setup, including the probe-to-probe capacitance. The additional sources of the parasitic feedthrough currents are the pad-to-substrate capacitance, the pcb parasitic capacitance, and the fringing field induced parasitic capacitance (usually comparatively small).

To remove the parasitic effects from the sensor output, the carrier demodulation technique was used, [33]. For that purpose, a high-frequency carrier signal of 100 kHz and amplitude of 0.5 V was applied to the structure in addition to the driving signal. The carrier signal was multiplied by the time-varying sense capacitance of the resonating structure, resulting in motional current, frequency-shifted to sidebands around the carrier frequency and separated from the parasitic feedthrough currents at the drive frequency. The bandpass filtering was then applied to eliminate the low frequency parasitic feedthrough component. The subsequent demodulation back down to the resonance frequency yielded in a signal cleared from parasitic currents.

The described carrier demodulation technique was applied for frequency response characterization of the sensor with electrical connection through top electrodes, and through vias. Frequency sweeps, obtained using different electrical connection methods, showed a good match, indicating that the parasitic effects were successfully removed in both experiments, Fig. 17.

In order to evaluate the difference in sensor performance after introducing vias, two TRG prototypes of the same design were tested: a sample fabricated using a conventional SOI process without vias and a sample fabricated using the TWIDS process. In both cases, the method of sensor excitation/detection thru the top electrodes, wire-bonded to the gold pads of an LCC package, was utilized. The transfer function analysis, presented in Section IV B, was then performed to estimate the value of total parasitic capacitance in parallel with the sensor, Equation (3). The values of parasitic

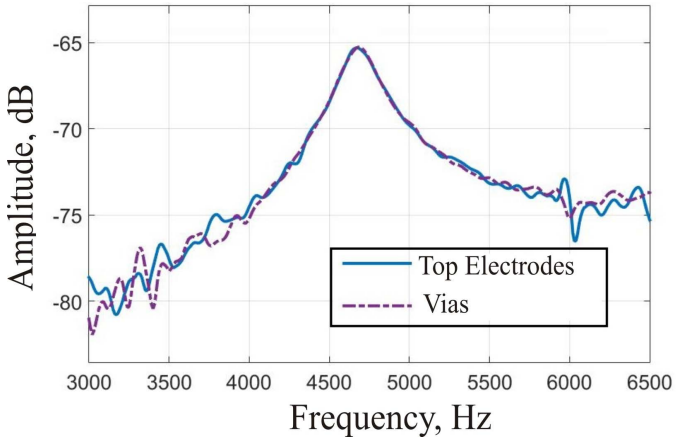

Fig. 17. Frequency sweeps, obtained using carrier demodulation technique, showed a good match between excitation/detection thru device-side (top electrodes) and interconnect side (vias).

capacitance C_p of 0.3 pF and 0.21 pF, correspondingly, were extracted for the sensor with and without vias. From this experiment, the conclusion was made that although the via process introduced additional parasitic capacitance in parallel with the sensor, its value was relatively low and did not result in significant loss of signal, less than 1.2 dB.

V. Mechanical Stability

Some limitations of the TWIDS technology are related to mechanical stability of the structure, that can be compromised due to a high-density array of insulating air gaps. The wafer-level mechanical reliability during processing is a concern because once the integrity is lost, the wafers are prone to breakage, [34]. In order to avoid wafer cracking during the sensors dry etching step, the handle side of the wafer was attached to a silicon carrier using a thin layer of thermal grease. The mechanical reliability of individual dies at the packaging assembly level, as well as during shock and vibrations, is also an important issue.

The solution is sought in filling the insulating trenches by a dielectric material, such as Parylene C or silicon nitride. The choice of the filling material depends on vias applications and is a trade-off between the electrical, thermal, and mechanical properties of the interconnects. Parylene C, which has low relative permittivity of 3.1, is a good candidate for gaps filling. It is applied at room temperature and does not introduce any concerns for thermomechanical reliability of copper via. Moreover, Parylene deposition rate (about 5 μm/hr) is comparatively high, making it a suitable material for filling even large gaps (up to 35 μm).

Finite Element Method (FEM) was used to study the mechanical stability of via with the air gap and the insulator-filled gap. The simulation was conducted in COMSOL Multiphysics, in which a solid mechanics physics and time-dependent study were selected. The geometries and material properties were manually defined in COMSOL. A model of a 3.3 mm by 3.3 mm silicon die with 600 μm thickness and 315 μm spacing between the vias was built. Mechanical properties of the materials used for the FEM study are summarized

TABLE II
MECHANICAL PROPERTIES OF MATERIALS

	Youngs Modulus (GPa)	Density (kg/m^3)	Poisson Ratio	Yield Stress (MPa)
Silicon	170	2329	0.28	7000
SiO2	70	2200	0.17	155
Si3N4	250	3100	0.23	500
Gold-Tin (eutectic solder)	68	14700	0.405	275
Copper (electro-plated)	120	8900	0.34	200
Parylene C	2.758	1289	0.4	70

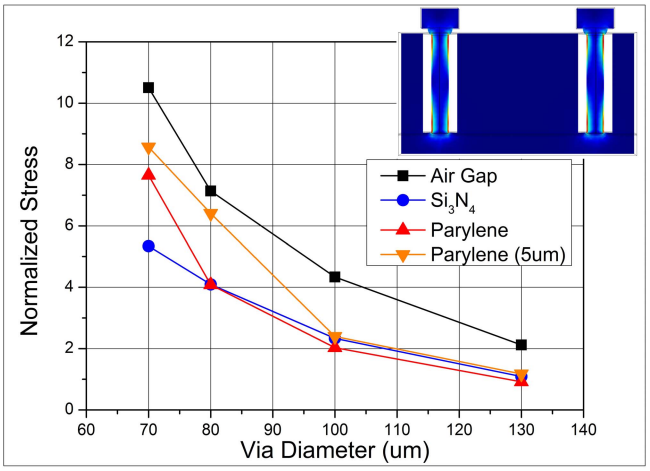

Fig. 18. Normalized principle stress in a die under 15000 g shock as a function of via diameter.

in Table II. Within the solid mechanics physics module of COMSOL, the linear elastic material properties were used.

Stress distributions under mechanical shock with the amplitude of 15,000 g were calculated for via diameter in the range from 70 μm to 130 μm. We considered three cases: via with the 35 μm air gap, via with the gap fully filled with Parylene C or silicon nitride, and via with the gap partially filled with Parylene, Fig. 18. In all cases, a silicon die is attached to a fixed constraint using eutectic solder ball. Simulations showed that the maximum stresses are located at the point of via attachment to the contact pad and at the bonding interface, Fig. 18 (insert). Presented data is normalized to the values for the solid silicon die without via. The maximum stress of a die without via appears at the silicon-eutectic solder interface. Our study revealed that, for example, in the case of a 100 μm diameter via, filling the gaps with parylene allows for reducing the stresses at the bonding interface by more than 2.1 times.

Reduction of via diameter is necessary for the small diameter contact pads of the miniature devices; however, it leads to a significantly increased stresses in the structure, Fig. 18. Filling of the air-gap improves the mechanical stability of the vias. According to FEA, in the case of a 70 μm diameter via, filling the gaps with nitride is the most effective way of via reinforcement. Shock survivability improved from 5,000g to 10,000g, while the parylene-filling only improved it to

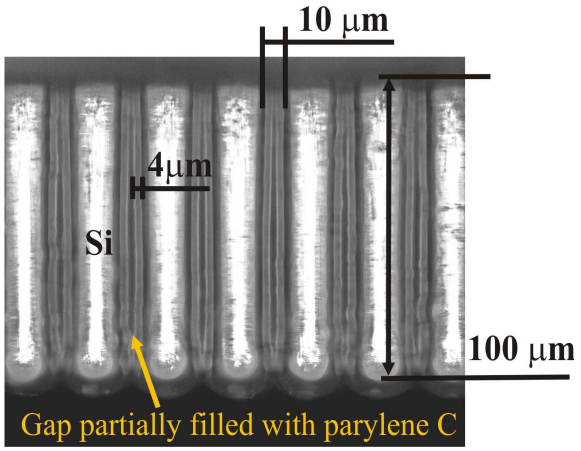

Fig. 19. 10 μm insulating gaps partially filled with parylene C.

TABLE III
PROCESS PARAMETERS FOR PARYLENE C DEPOSITION

Parameter	Value	Units
Vaporization Temperature	175	°C
Pyrolysis Temperature	690	°C
Deposition Temperature	25	°C
Deposition Pressure	25	mTorr
Grams of dimer	10	g
Gap width	10	μm
Thickness Deposited	4	μm

7,500g. Simulation results suggest that for the via diameter of 100 μm and larger, all the filling methods are suitable for reinforcement. In the case of a 100 μm diameter via, for example, either of these methods results in improvement of shock survivability up to 23,000g. However, filling gaps with parylene is a preferable method of vias reinforcement due to a significantly faster deposition rate and lower deposition temperature as compared to silicon nitride.

Fig. 19 shows the 10 μm insulating gaps partially filled with parylene C. The conformal parylene-C film was deposited using the SCS PDS 2010 tool from Specialty Coating Systems, Inc. The process parameters for parylene deposition are summarized in Table II. An adhesion promoter, Silane A-174, was applied to the sample before deposition. A wafer with DRIE preetched insulating gaps was placed in the middle of the deposition chamber and, using 10 grams of dimer material, approximately 4 μm of parylene-C was deposited inside the 10 μm trench and 4.5 μm on the top surface. Prior to parylene deposition, the device" side of the wafer was masked with photoresist and covered with dicing tape. After the gaps filling step, the entire parylene film was peeled off along with the dicing tape and the photoresist was removed in acetone.

As previously discussed in this paper, filling of gaps results in an increased parasitic capacitance of interconnects, which may lead to signal degradation, especially in high frequency applications. In this case, an alternative approach where gaps are only partially filled with insulating material can be utilized. For example, in the case of a 100 μm diameter via, partial filling of the gaps with Parylene C (5 μm on each sidewall)

allows for 1.55x improvement in mechanical stability without a significant increase in via parasitic capacitance value (by less than 22 fF).

Another limitation of the presented TWIDS technology is related to vias thermal reliability. Potential thermal reliability issues are associated with Cu diffusion in Si and Si oxide at high temperatures (>300 °C, [35]), as well as the thermal stresses in Cu via. The samples characterized in this paper, were annealed at 110-150 °C during the silicon dry etch step, which is within the temperature range requirements for consumer and automotive grade gyroscopes (−40+105 °C). However, if high temperature processing steps follow the vias fabrication, a different type of vias might be considered in this case, such as single-crystal silicon or polysilicon vias.

VI. Conclusion

A new approach for co-fabrication of MEMS sensors and high-aspect ratio low-resistance vertical interconnects in thick SOI wafers (TWIDS process) was presented. The method is based on bottom-up seedless copper electroplating of through-wafer vias, using a highly doped device layer of an SOI wafer as a seed. The described process allows for voids free features, low resistance (< 100 mΩ), and high aspect ratio (wafer thickness to copper diameter up to 10:1). Through-wafer interconnects are particularly appropriate for integration with SOI sensors, such as gyroscopes, accelerometers, and resonators. The TWI technology presented in the paper may find applications in RF-MEMS devices, where ultra-low resistance and low parasitic capacitance interconnects are typically required for reduction of signal losses, [31].

For the purpose of technology demonstration, prototypes of an SOI MEMS toroidal ring gyroscope with 6:1 aspect ratio interconnects were fabricated using TWIDS process. Sensors experimental characterization showed that TWIDS allow for low parasitic losses and are suitable for miniature capacitive sensors.

Furthermore, we investigated mechanical stability of interconnects with air gap and insulator-filled gap under 15,000 g shock. We demonstrated that partial filling of the gaps with Parylene C allows for 1.55× improvement in structural rigidity without a significant increase in via parasitic capacitance value.

Due to the high aspect-ratio, low resistance and low parasitic capacitance, TWIDS technology may find a wide scope of applications, including 3D packaging of MEMS inertial sensors and RF MEMS.

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