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Fluxless Bonding of Silicon to Alumina Substrate Using Electroplated Eutectic Au-Sn Solder

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Abstract

Large 6mm x 9mm silicon dice have been successfully bonded on alumina substrate with electroplated Au80Sn20 eutectic alloy. Eutectic AuSn is one of the best known hard solders having excellent fatigue-resistance and mechanical properties. A fluxless bonding process in 50militorrs of vacuum environment is presented. Vacuum environment is employed to prevent tin oxidation during the process. The oxygen content is expected to be reduced by a factor of 15,200, comparing to bonding in air. One of the challenges in silicon-to-alumina bonding is the large mismatch in thermal expansion between silicon of 2.7×10^{-6}ppm/°C and alumina of 7×10^{-6}ppm/°C. Electroplating method is used to build multi-layer solder. It is an economical alternative to vacuum deposition method and can produce thick solders. Joints fabricated are examined using Scanning Electron Microscope (SEM), and Energy Dispersive X-ray Spectroscopy (EDX). It is found that proper bonding condition is needed to turn the stacked layers into a uniform AuSn eutectic alloy. Nearly void-free joints are achieved and confirmed by a Scanning Acoustic Microscope (SAM). To evaluate the reliability of the solder joint and the bonded structure, samples will go through thermal cycling test to determine failure modes. Microstructural changes of the solder joints during thermal cycling test will also be investigated.

1. Introduction

Many semiconductor device chips are bonded to ceramic (alumina) substrates using solders. Popular solders in the industry are soft solders such as eutectic SnPb, SnAg and SnCu. These solders have relatively low melting temperature and high thermal conductivity. However, they are not mechanically strong and are likely to incur thermal fatigue and creep [1]. The eutectic Au80Sn20 alloy, which is a hard solder, has been widely used in photonic packaging due to its high mechanical strength and free of thermal fatigue and free of creep [2-4]. One difficulty in using eutectic AuSn solder is that the parts to be bonded must have relatively close thermal expansion coefficient because its range of plastic strain is very small. Thus, it has always been a challenge to bond large silicon chips to alumina substrates because of thermal expansion mismatch, 2.7×10^{-6}ppm/°C for silicon versus 7×10^{-6}ppm/°C for alumina. We had previously demonstrated this possibility using AuSn preform without using any flux [2].

In this work, we look into electroplating processes to fabricate the solder structure directly on the alumina substrates. The solder structure is designed so that the bonding process can be performed without the use of any flux. Fluxless feature is critically important in achieving void-free joints in bonding large chips because flux and residues can be easily trapped in the joint, causing voids. Fluxless technique has become more important because there are more devices such as MEMS and photonic that cannot accept flux. In some applications, flux residues could cause reliability problem, if not completely removed [5].

Au-Sn alloys can be produced in several ways such as the use of solder preforms, vacuum deposition technique, and electroplating method. Solder preforms, popular for some applications, have difficulty in alignment and get oxidized easily before and during bonding [6]. Thermal (or electron-beam) evaporation in high vacuum can deposit metal thin films that are very clean and uniform with excellent thickness control. Thermal evaporation in vacuum also makes it possible to inhibit tin oxidation during the deposition process, and thus allow the tin layer to be capped with an oxygen barrier layer such as gold in the same vacuum cycle [7]. However, the deposition process and equipment maintenance are costly for making thick layers such as 10 μm and above. To find an economical alternative, we turn to the electroplating processes. An additional advantage of electroplating is its low process temperature (room temperature~60°C) that reduces unwanted diffusion and reaction between Au and Sn, which are more likely to occur in vacuum deposition process due to higher substrate temperature. The use of electroplating processes makes patterning of solder structure possible.

In the first step of our fluxless bonding processes, 11μm Au is electroplated over 10mm x 12mm alumina substrate, followed by 7.5μm Sn with 0.1μm Au capping layer for achieving eutectic composition. The thin Au capping layer, when electroplated, reacts with Sn to form $AuSn_4$ intermetallic compound immediately and works to prevent oxidation of inner Sn to achieve fluxless feature as proven in our previous research [8, 9]. The silicon chips, 6mm x 9mm in size, are coated with 0.03μm Cr and 0.1μm Au deposited in vacuum. Cr act as an adhesion layer and Au layer is to prevent Cr oxidation. Bonding is performed in a vacuum chamber that can be pumped to 50 militorrs. Three bonding conditions are used and compared. In the first method, fluxless bonding is conducted at 320°C. Secondly, bonding is performed at higher process temperature of about 430°C without reflow. Lastly, electroplated alumina substrate is loaded in a vacuum chamber and undergoes a reflow process at temperature above 430°C, followed by 320°C bonding process to silicon chips. Higher temperature is used for second and third method to ensure that the plated Au-Sn-Au structure turns into a mixture containing adequate

molten phase during the bonding. All processes are done without using any flux. i.e. flux-free.

In this paper, we report our success in fluxless bonding technique between silicon chip and alumina substrate using electroplated eutectic Au80Sn20 structures. The fluxless bonding process in vacuum environment and resulting joint are presented. SEM and SAM were used to evaluate the quality of the joint. To evaluate the reliability of the solder joint and the bonded structure, samples will go through thermal cycling test. Microstructural changes of the solder joints during thermal cycling test will be investigated and assessed.

We first present Gold-Tin binary system for better understanding. Experimental design and procedures are described. Experimental results are reported and discussed. A short summary with future plan is then given.

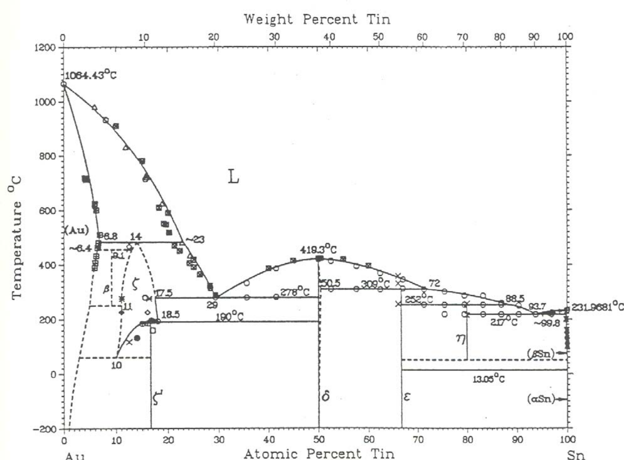


Figure 1 - Tin-Gold phase diagram [10]

2. Gold-Tin Binary System

The gold-tin phase diagram [10] as shown in Figure 1 depicts a complex combination of eutectic and peritectic systems. Gold-tin alloy system is so complicated with five intermediate phases appearing: ζ phase, Au_5Sn, AuSn, $AuSn_2$, and $AuSn_4$. The ζ phase (hexagonal close-packed crystal structure) is homogeneous between 12 and 16 at. % Sn. The intermetallic compound AuSn (hexagonal NiAs structure) has a very narrow range of solubility. The homogeneity range of $AuSn_2$ (orthorhombic) and $AuSn_4$ (orthorhombic $PtSn_4$ structure) are also very narrow. First, the liquid phase is identified as L. Second, the L $\leftrightarrow$ [ζ + AuSn] eutectic occurs at 278°C with 29.5 at. % Sn. This is the most commonly used eutectic of 20 wt.% Sn and 80 wt.% Au. Third, the δ phase is determined as the AuSn intermetallic that has a melting point of 419.3°C. The homogeneity range extends from 50.0 to 50.5 at.% Sn. Fourth, the ε phase is identified at the $AuSn_2$ intermetallic compound. The temperature of the peritectic [L + δ] $\leftrightarrow$ ε reaction is 309°C, giving the liquidus composition of about 72 at.% Sn. The homogeneity range of this phase is very narrow. Fifth, the η phase is found to be as the $AuSn_4$ compound. The temperature of the peritectic [L + ε] $\leftrightarrow$ η reaction is 252ºC, giving the liquidus composition of about 88.5 at.% Sn. The L $\leftrightarrow$ [η + βSn] eutectic reaction occurs at 93.7 at.% Sn at 217ºC, called as second eutectic reaction. Lastly, the allotropic temperature between two terminal solid solutions of (β-Sn) and (α-Sn) is 13.05ºC. The (β-Sn) solid solution has a solubility up to 0.2 at. % Au in β-Sn. The (α-Sn) solid solution has a very limited solid solubility, that is, less than 0.006 at. % Au in α-Sn.

3. Experimental Procedure

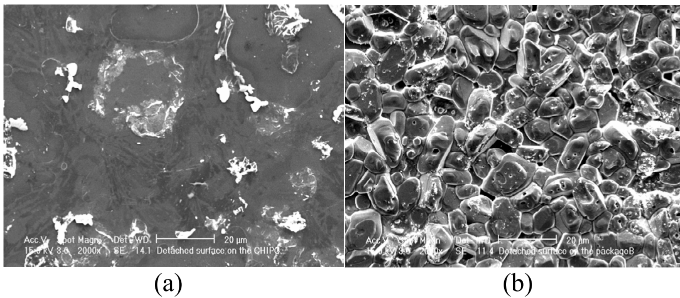
To perform fluxless bonding, thin Cr layer of 0.03 μm and Au layer of 0.1 μm are deposited on a Si wafer in a high vacuum e-beam evaporator (3×10^{-6} torr). Cr acts as an adhesion layer and the Au layer is to prevent Cr oxidation. The wafer with Cr/Au layers is diced into 6 mm x 9 mm pieces using Tempress dicing saw. Alumina substrate with Ti/W/Au metallization is first electroplated with 11μm of Au. The Au plating bath is neutral non-cyanide plating solution at pH 7 based on sulfite complex with mild agitation. The current density and process temperature were 4.6mA/cm^2 and 60°C, respectively. It is then followed by 7.5μm of Sn plating in a stannous tin based bath at 21.5mA/cm^2. Very thin Au capping layer (0.1μm) is plated over alumina/Au/Sn substrate mainly to prevent the oxidation of the Sn. To prevent Sn oxidation prior to gold capping layer plating, the sample is rinsed in acid solution right after Sn plating. The alumina substrate is diced into 10mm x 12mm. The Si chip and alumina substrate are held together with a static pressure of 50 psi (0.35 Mpa) using a graphite fixture to ensure intimate contact. The assembly is then loaded into a vacuum chamber built in house and pumped down to 50 militorr vacuum environments. The furnace is turned on and the temperature of the fixture is monitored with a thermocouple. Three bonding conditions are employed. First, the vacuum chamber is heated to optimum temperature for bonding, 320°C using a temperature controller. The assembly was then allowed to cool naturally to room temperature in vacuum ambient. Secondly, bonding is conducted at higher process temperature of 430ºC in the same vacuum ambient. Bonding time is much longer than that of the first condition. In third method, the alumina substrate (alumina/Au/Sn/Au) undergoes a reflow process at 430ºC, followed by fluxless bonding at 320ºC. To evaluate the quality of the joints, SAM was used to identify voids in the solder joints. SEM and EDX were employed to characterize the composition and microstructures of solder joints. Re-melting temperatures of several samples are to be measured by de-bonding test.

4. Experimental Results and Discussions

A. 320ºC bonding process – bonding failure

Si chip and alumina substrate were detached after bonding process at 320ºC. Figure 2 displays secondary electron images on the detached surface of si side and alumina side, respectively. On Si side, mainly Si with little amount of Cr is detected by EDX analysis, while certain type of AuSn intermetallic compounds were detected on alumina side. This reveals that broken interface is between Si/Cr and AuSn intermetallic compound. Process temperature of 320ºC seems not high enough to liquefy the whole solder joint, but only partly dissolves the joint. Three

stacked electroplating layers of Au/Sn/Au need to react each other during the bonding process to reach a uniform composition of Au80Sn20, but some portion of the joints still remains as a solid material, and cannot be attached to silicon chip leading to a bonding failure. To reach a uniform composition of eutectic Au80Sn20, Sn has to pass through some intermediate phases such as $AuSn_4$, $AuSn_2$, and AuSn while Sn is diffusing into Au layer. $AuSn_2$ and $AuSn_4$ are expected to melt below 320ºC, but AuSn does not melt at our process temperature. The melting temperature of AuSn intermetallic compound (δ phase) is 419ºC, and it is obvious that 320ºC process temperature is too low, providing the existence of AuSn intermetallic compound. Thus, higher process temperature is desired to ensure that the plated Au-Sn-Au structure turns into a mixture containing adequate molten phase during the bonding.

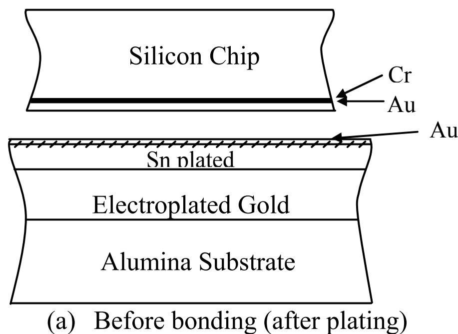


(a) (b)

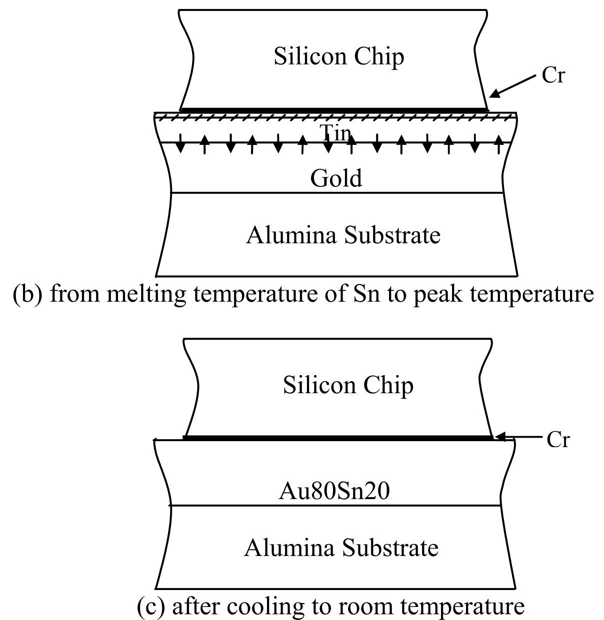
Figure 2 - Top view of the detached sample after 320ºC bonding process (a) Si side (b) alumina side

B. 430ºC bonding process

Based upon the results that we got from 320ºC bonding process, we move to much higher process temperature of 430ºC. Above 419ºC, all major three AuSn intermetallic compounds are to be dissolved; AuSn (419ºC), $AuSn_2$ (309º) and $AuSn_4$ (252ºC). High enough temperature and long enough reflow time enable the joint to become a very uniform composition of Au80Sn20. As shown in Figure 3(b), as the temperature reaches 232ºC of Sn melting temperature, Sn starts to melt to react with Au layer below and generate several kinds of AuSn intermetallic compounds. As the temperature further increases to peak temperature of 430ºC, all the possible compound layers are dissolved to react with Si chip to form a strong joint. After cooling down to room temperature, the joint eventually becomes very strong as displayed in Figure 3 (c).



(a) Before bonding (after plating)



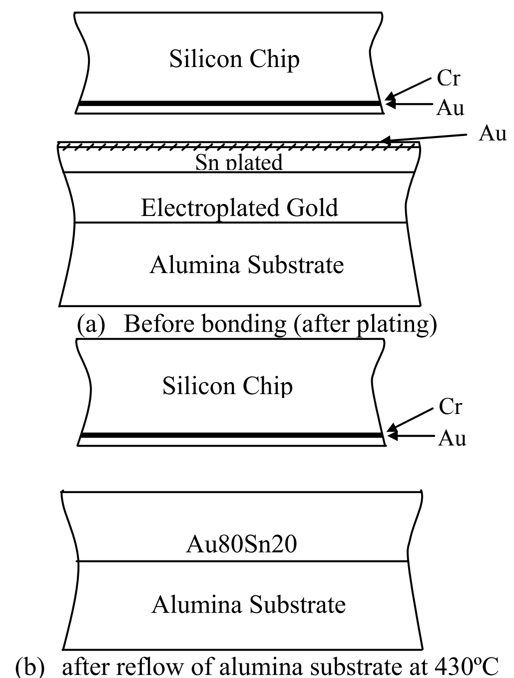
(b) from melting temperature of Sn to peak temperature

(c) after cooling to room temperature

Figure 3 - Principle of the fluxless bonding at 430ºC

C. 320ºC bonding after reflow process at 430ºC

We propose another way to bond silicon chip to alumina substrate. The sample undergoes a reflow process at 430ºC, followed by bonding at 320ºC. Electroplated alumina substrate is reflowed inside a vacuum chamber at 430ºC to turn the stacking layer structure of Au/Sn/Au into uniformly distributed eutectic AuSn alloy as shown in Figure 4 (b). This substrate and si chip are held together for fluxless bonding conducted at 320ºC, about 40ºC higher than eutectic AuSn melting temperature. Final joint is displayed in Figure 4(d).



(a) Before bonding (after plating)

(b) after reflow of alumina substrate at 430ºC

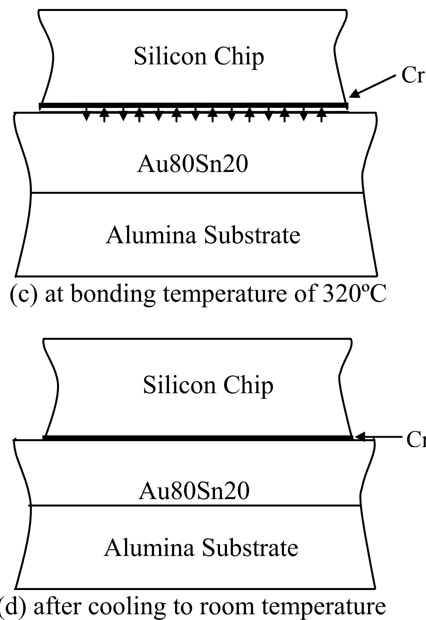


Figure 4 - Principle of the fluxless bonding at 320ºC after reflow process at 430ºC

D. Joint analysis by SEM and SAM

Figure 5 shows secondary electron image of the joint with lower magnification (a) and higher magnification (b). Nearly perfect joint without any big void is shown. Solder layer thickness is down to about 3μm due to applied high pressure during the bonding process. EDX data shows that final joint composition is very close to eutectic Au80Sn20.

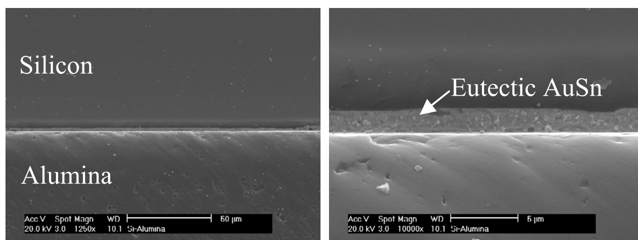


Figure 5. SEM image of the joint at (a) low magnification (x1,250) and (b) high magnification (10,000x)

The Transmission SAM analysis was performed on samples of eutectic AuSn joint to evaluate the quality of the joint. The SAM operates at an acoustic frequency between 100~150 MHz. This is very useful for non-destructive testing of integrated circuit and optically opaque samples. The microscope has the ability to image internal features of a sample showing the presence of manufacturing and processing defects (voids). Voids are seen as high contrast images because of the mismatch in acoustic impedance between the solder material and the void. The acoustic image in Figure 6 shows that good quality joint with some small voids. We expect to produce nearly void-free joints with further effort to refine our processes. The solder joint is quite strong. We tried to break the joint with a hand tool but the silicon chip always broke first.

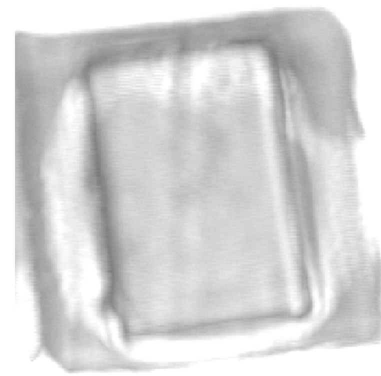


Figure 6 - SAM image of the eutectic AuSn joint

5. Summary

In summary, we have successfully developed fluxless bonding process between silicon chip and alumina substrate. Electroplating processes were employed to manufacture eutectic AuSn structures for achieving fluxless joints of high quality. Electroplated Au/Sn/Au layers on alumina substrate becomes a uniform eutectic AuSn composition either by high temperature bonding process or by reflow process before bonding. Electroplating method in fabricating thick solder layers is proven to be cost effective than the thermal evaporation technique in high vacuum. Another advantage of electroplating lies on the fact that very thicker films can be deposited. Proper choice of bonding layer and bonding condition can overcome the large mismatch in thermal expansion coefficient between silicon and alumina. This method and the use of electroplated eutectic AuSn offer the packaging industry a good economical alternative to other lead-free soft solders. This new fluxless process using electroplated eutectic AuSn structures could play an important role in various applications such as photonic devices, MEMS devices, sensor devices, and biomedical devices, where the use of fluxes is not allowed.

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